INCREASING SELF-TIMED CIRCUIT SOFT ERROR TOLERANCE

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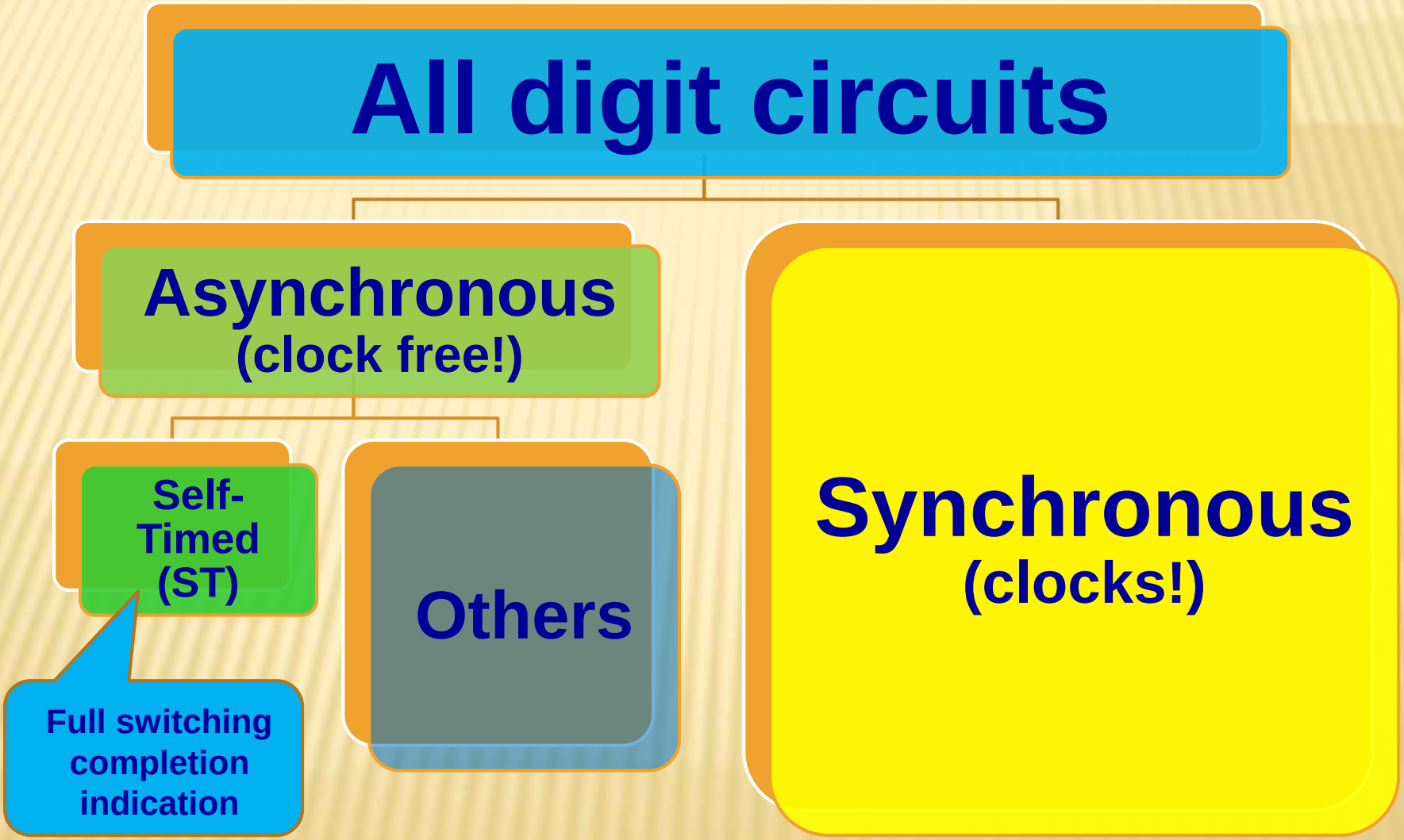
OUTLINE

- Synchronous and Self-Timed circuits
- Self-Timed circuit's soft-error tolerance
- Indication subcircuit implementation
- How to increase indication subcircuit immunity to soft-errors?
- Conclusions

CIRCUITS CLASSIFICATION



SELF-TIMED PRINCIPLES

- **Two operation phase:**
  - **work phase (data processing)**
  - **spacer (pause)**
- **Dual-rail information signal coding in combinational circuits**
- **Full indication of all circuit's cells in each operation phase**

ST CIRCUIT'S FEATURES

Advantages:

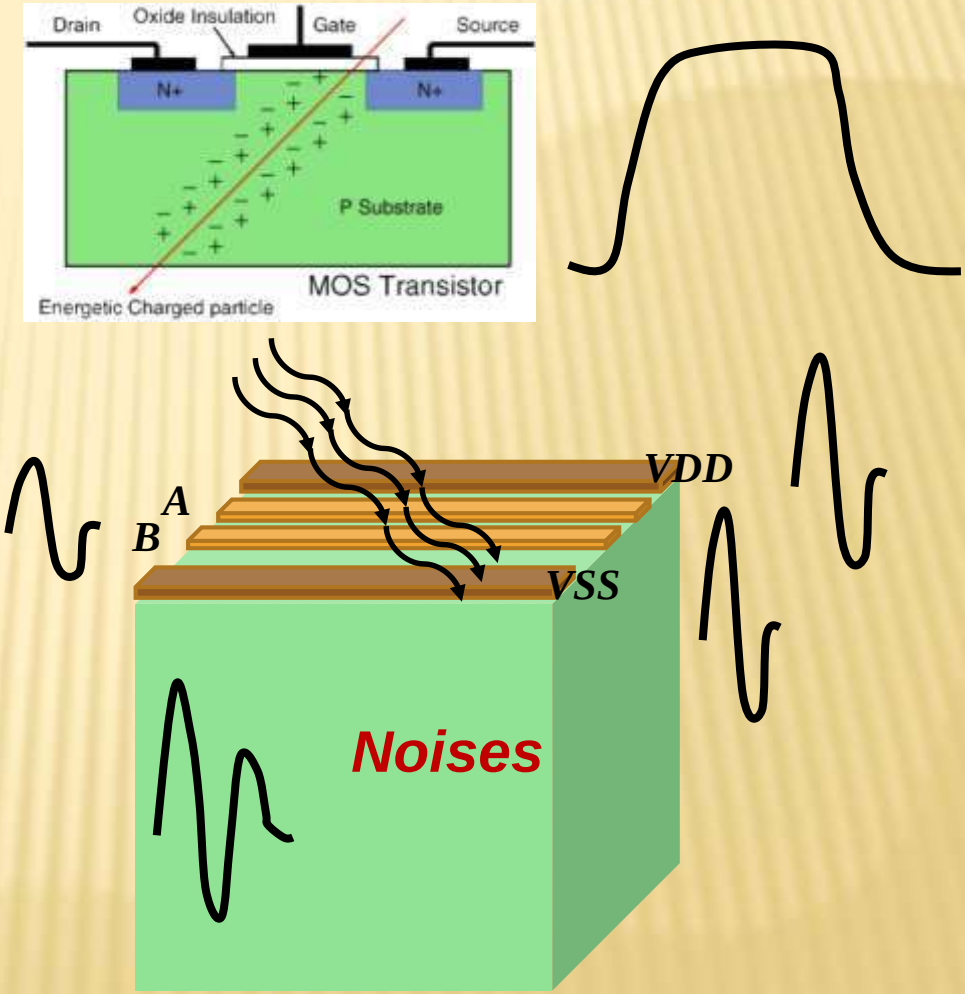
- Their workability does not depend on delay of their cells and wires
- Extremely wide workability range on supply voltage and ambient temperature,
- Constant failure detection and localization
- High soft error immunity

Draw-backs:

- Increased hardware complexity
- Lower performance in multi-bit data processing

SOFT ERROR SOURCES

- Nuclear particles and cosmic rays
- External electro-magnetic pulse
- Cross-talks on signal wires
- Noise on power stripes
- Substrate noises



DUAL-RAIL CODING

Two work states and one spacer

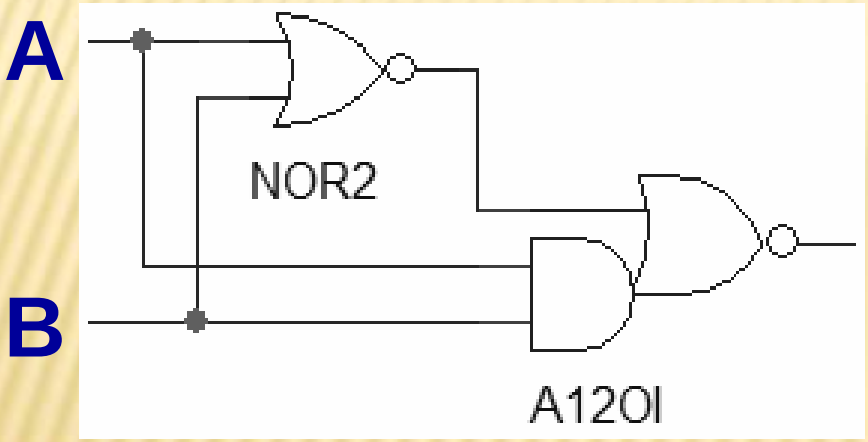
Dual-rail value	Spacer type	
	Null	Unit
01	Work state	Work state
10	Work state	Work state
00	Spacer	Anti-spacer
11	Anti-spacer	Spacer

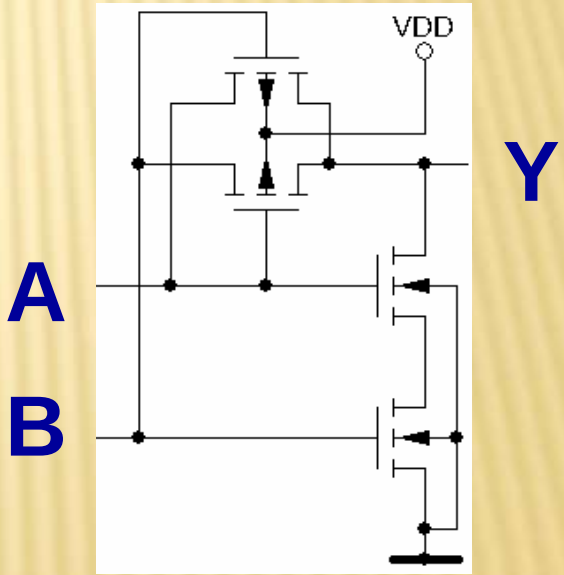
Anti-spacer is a state inverse to spacer. It is usually prohibited

INDICATION SUBCIRCUIT BASIS

Solution: ***Let's indicate anti-spacer as the second spacer by XOR / XNOR cell***

XOR circuitry





Standard cell basis **CMOS transistors basis**

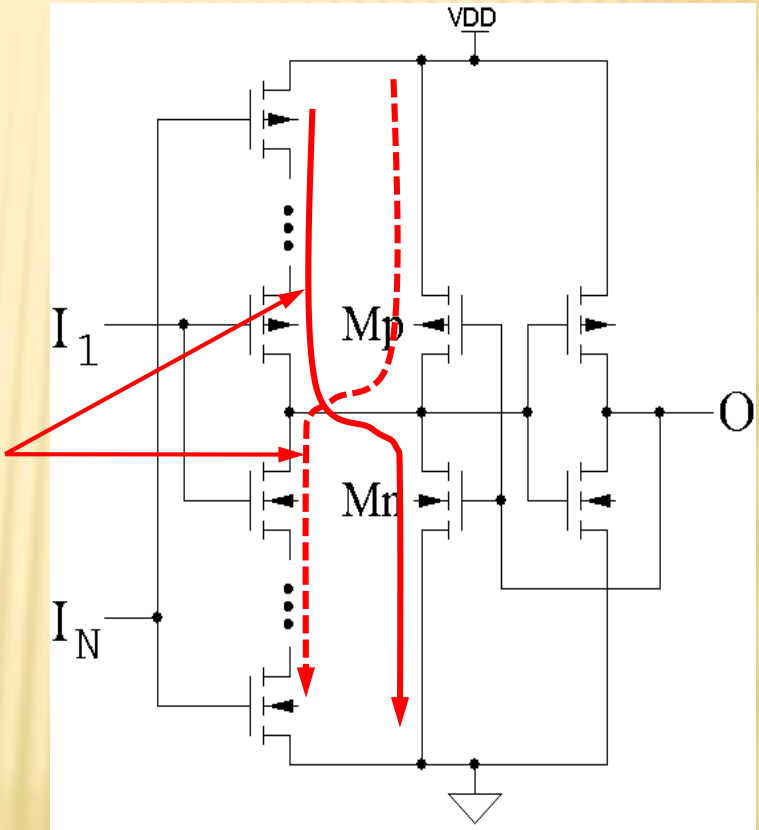
INDICATION CIRCUITRY

$$O^+ = I_1 \cdot I_2 \cdot \ldots \cdot I_N + O \cdot (I_1 + I_2 + \ldots + I_N)$$

Semi-static Muller's C-element:

+ Short-circuit current when switching

–Minimal complexity



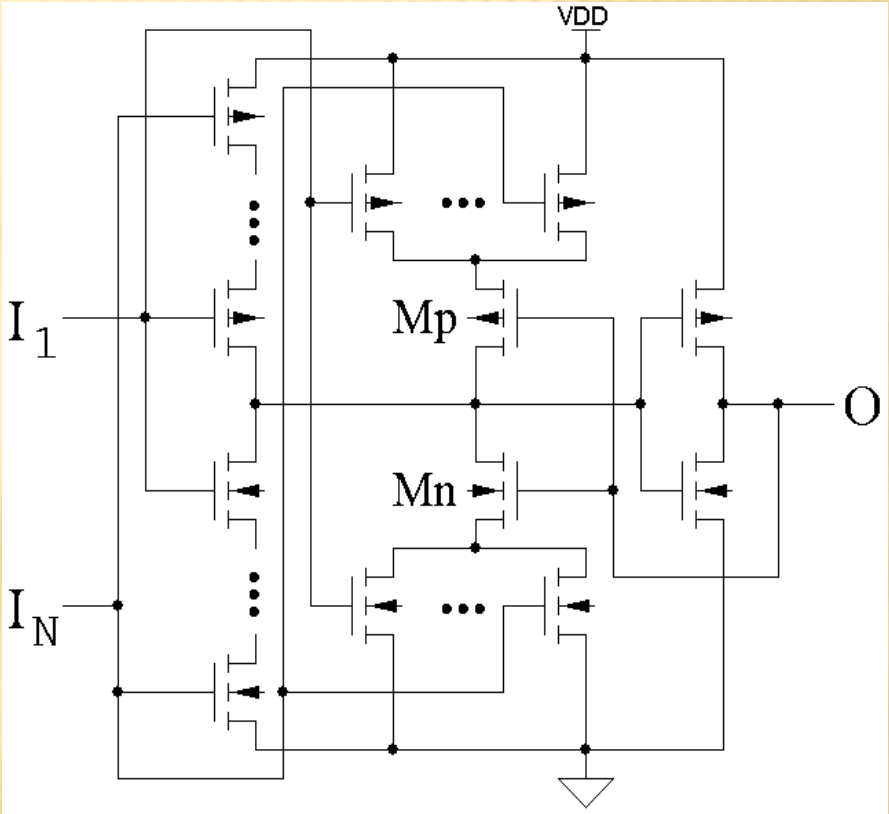
INDICATION CIRCUITRY

$$O^{+} = I_1 \cdot I_2 \cdot \ldots \cdot I_N + O \cdot (I_1 + I_2 + \ldots + I_N)$$

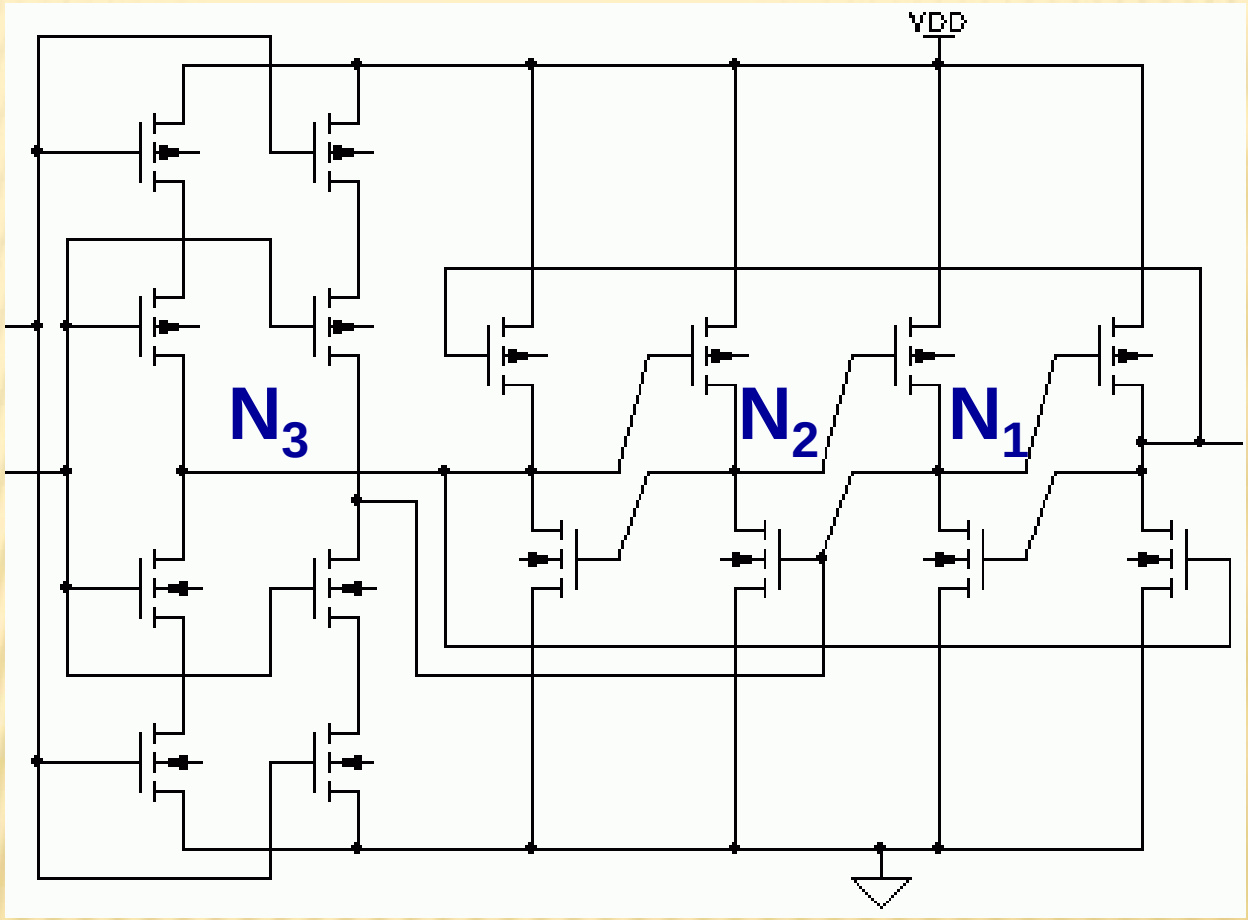
Static Muller's C-element or Hysteretic trigger:

+ Short-circuit current is absent

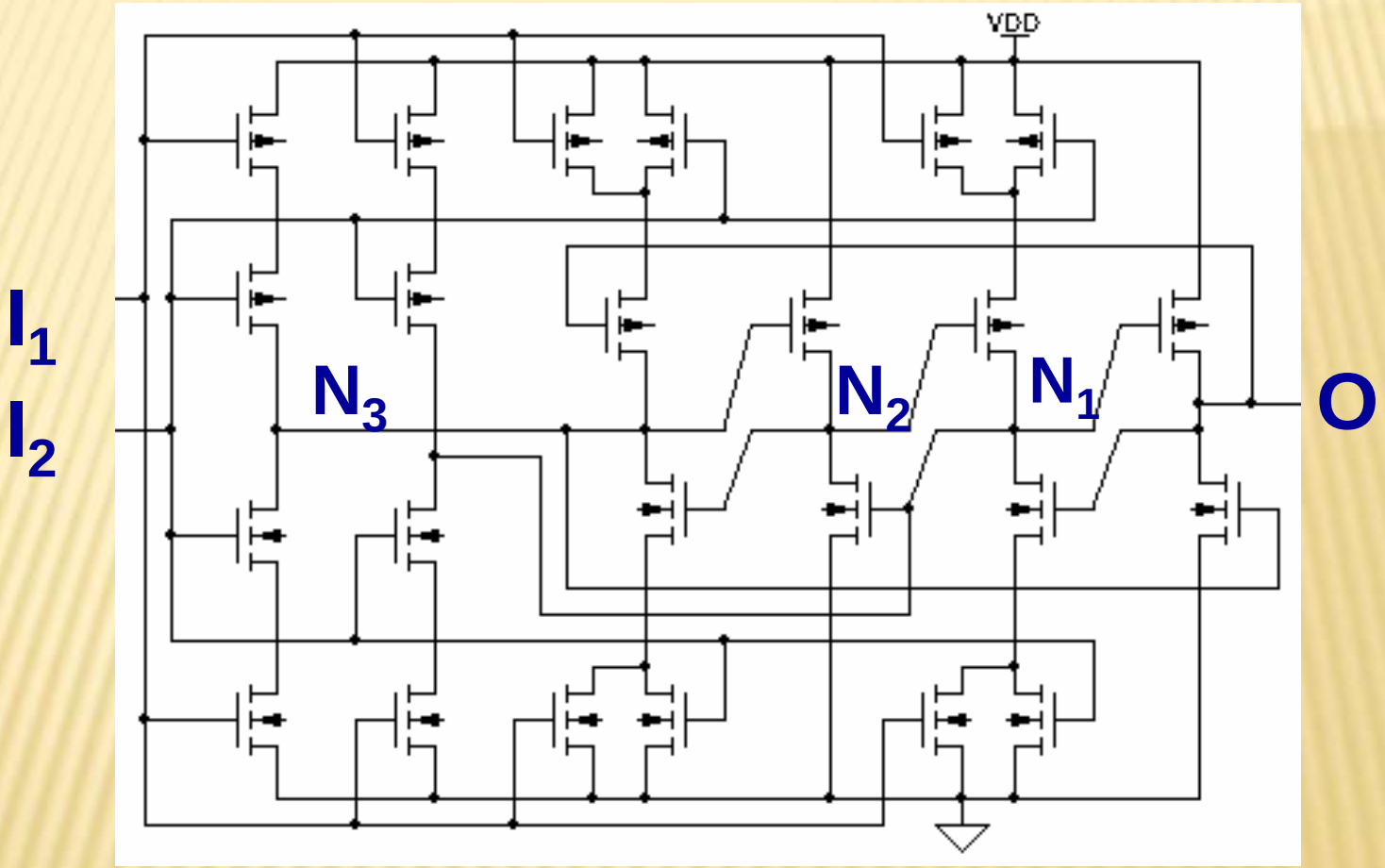
– Increased complexity



DICE-LIKE SEMI-STATIC C-ELEMENT



DICE-LIKE STATIC C-ELEMENT



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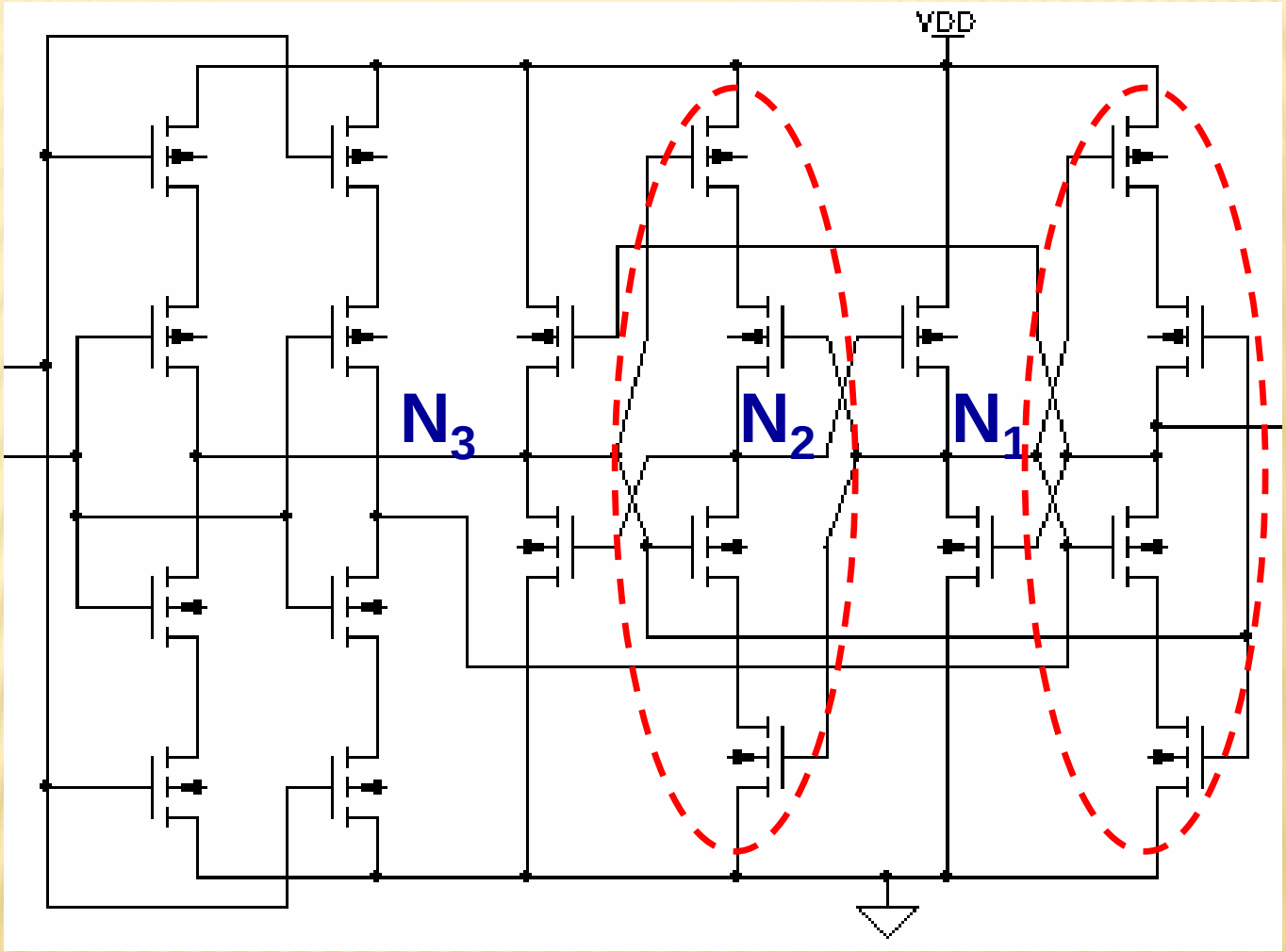

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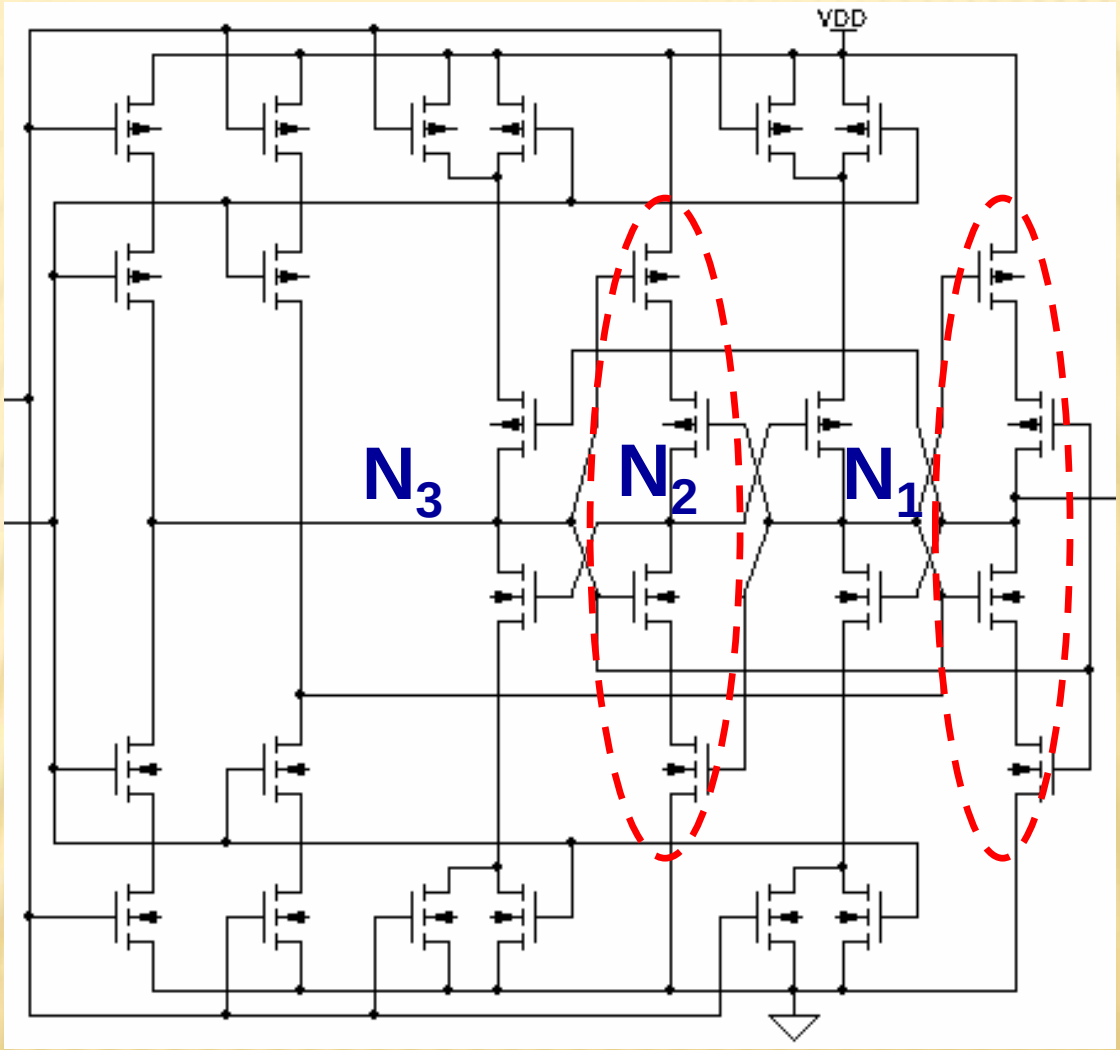
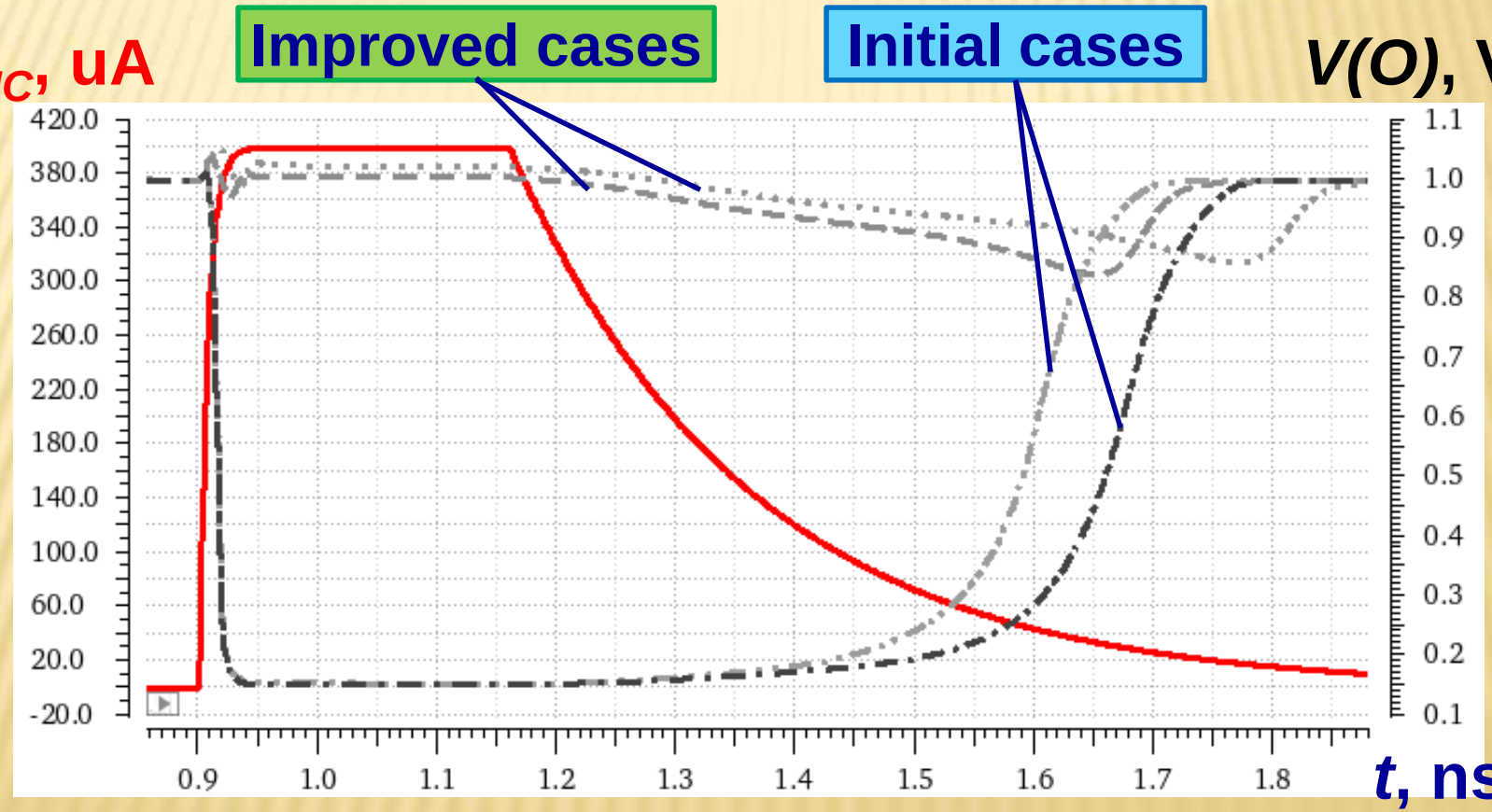


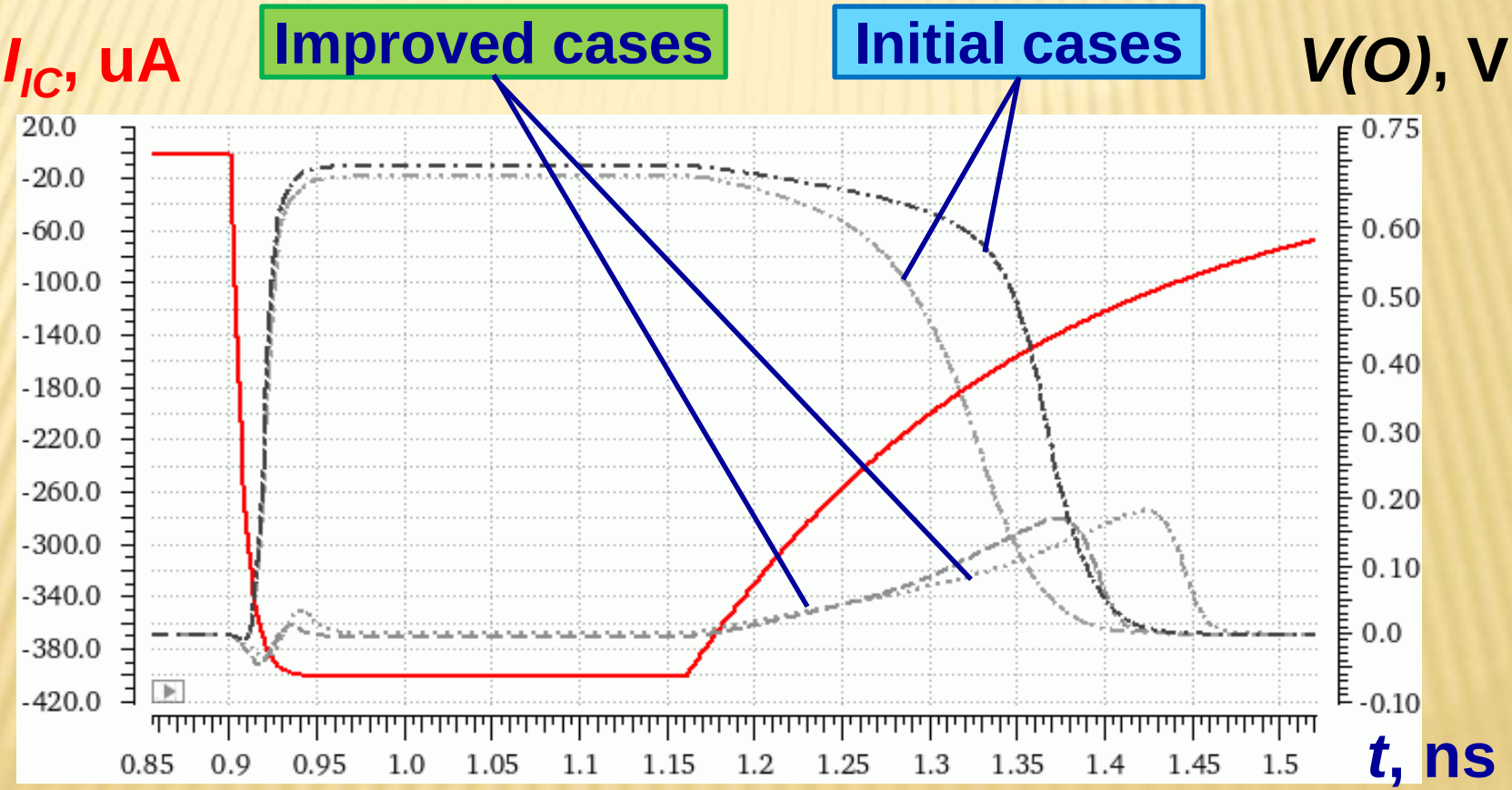
C-ELEMENTS COMPARISON (1)

The influence of ionization current pulse (A = 400 uA, t_R = 7 ps, t_F = 200 ps, "plateau" = 200 ps) at node N_1



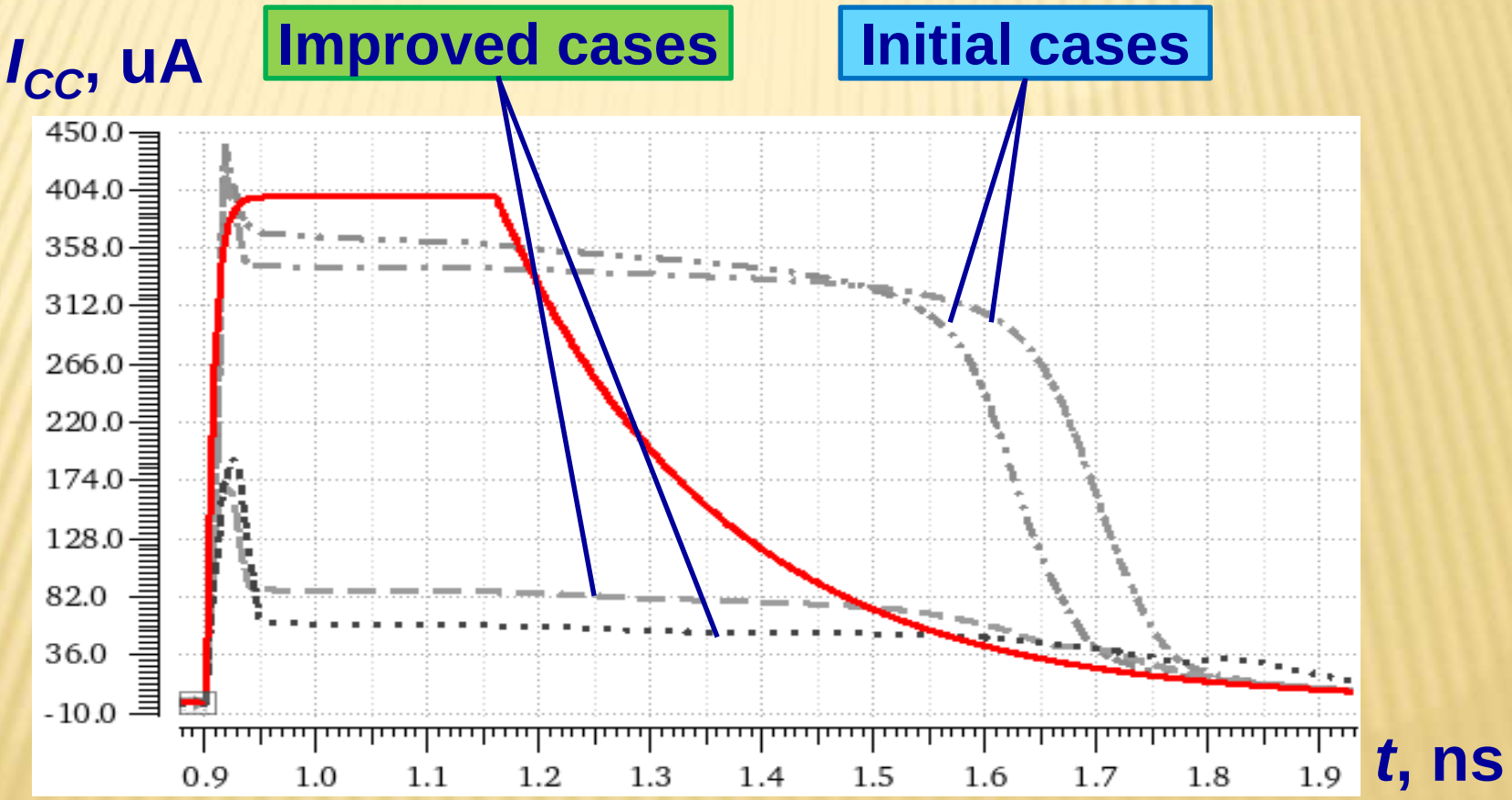
C-ELEMENTS COMPARISON (2)

The influence of ionization current pulse (A = –400 uA, t_F = 7 ps, t_R = 200 ps, "plateau" = 200 ps) at node N_3



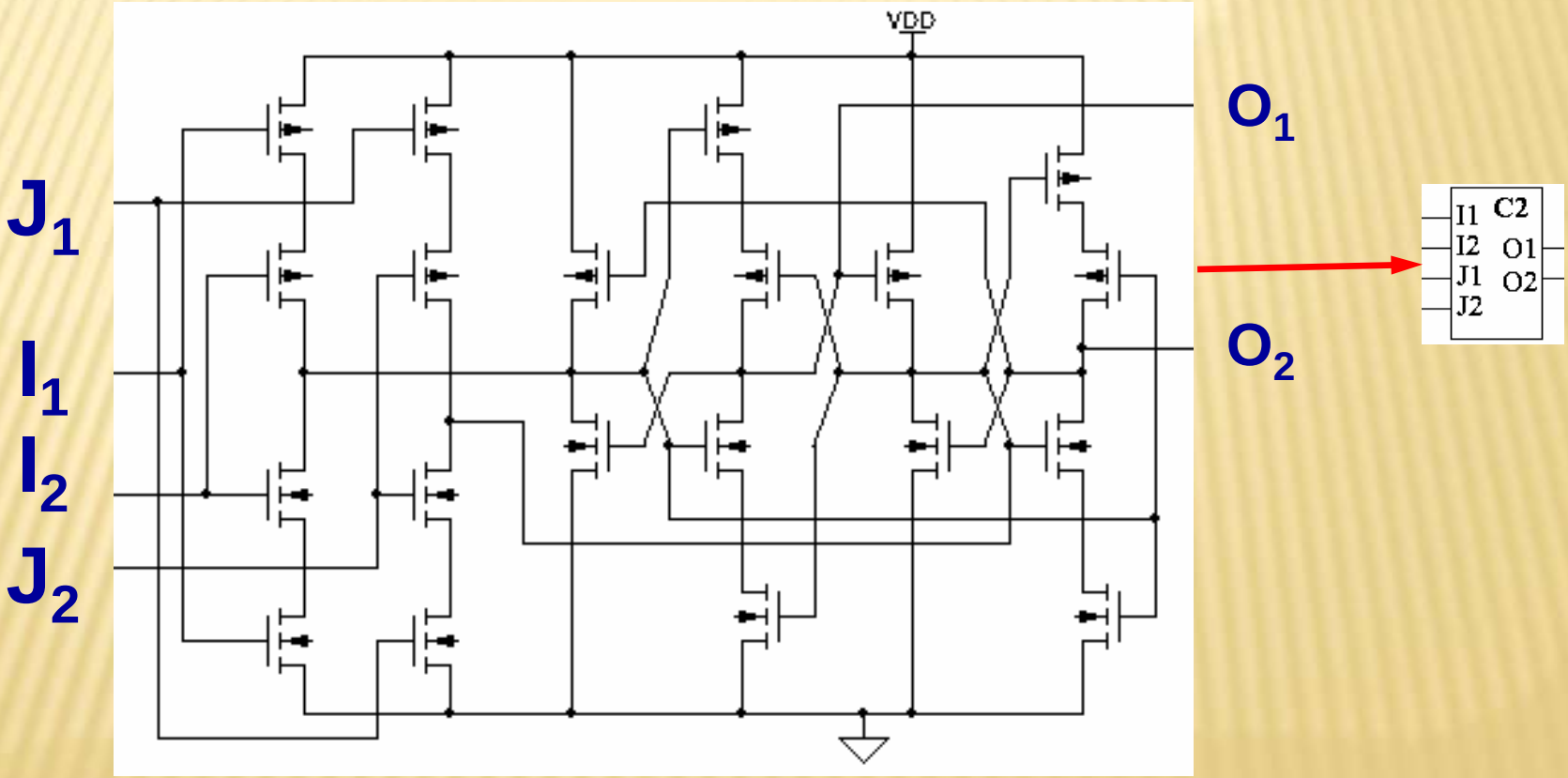
C-ELEMENTS COMPARISON (3)

Consumption current during soft error

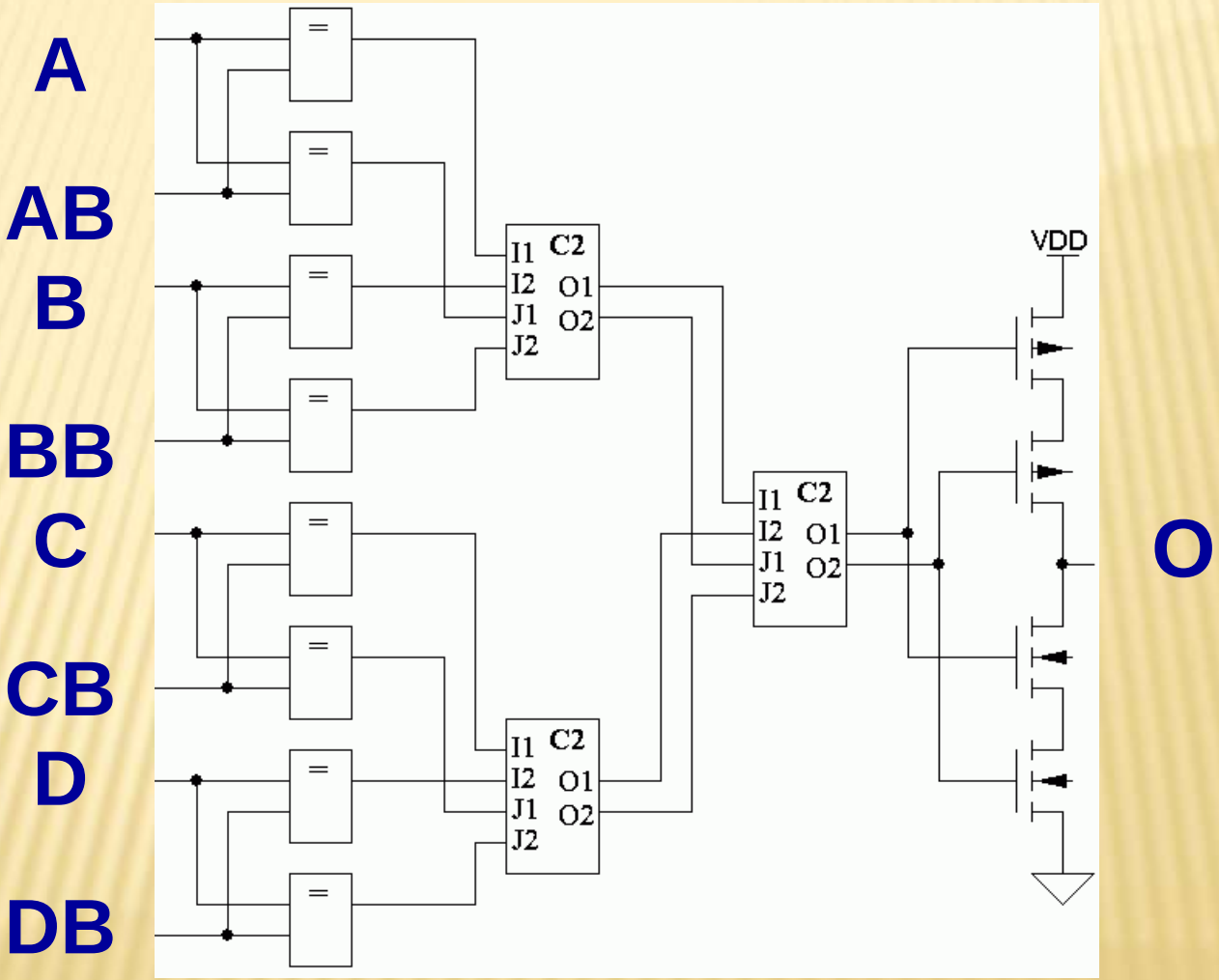


IN-PHASE C-ELEMENTS

C-element with in-phase input and output pairs masks soft error induced directly at any its output



INDICATION SUBCIRCUIT STRUCTURE



SUMMARY

- Soft error tolerance of the indication subcircuit largetly determines entire self-timed circuit's tolerance
- XOR or XNOR cells at the first stage of the indication subcircuit prevent the errors caused by anti-spacer state
- Four-transistor output cascade makes the DICE-like C-element entirely immune to single soft errors at its internal and input nodes
- The proposed indication subcircuit building technique doubles its hardware complexity but ensures its absolute immunity to the short-term soft errors

Thank You!

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