## IMPROVEMENT OF THE QUASI DELAY-INSENSITIVE PIPELINE NOISE IMMUNITY

Yuri A. Stepchenkov, <u>Anton N. Kamenskih</u>, Yuri G. Diachenko, Yuri V. Rogdestvenski, and Denis Y. Diachenko



Federal Research Center "Computer Science and Control" of Russian Academy of Sciences,

Perm National Research Polytechnic University

### CONTENTS

- Physical sources of soft errors
- Fail-safe discipline of QDI circuits
- Noise failure nature
- Register protection against stuck-at AS
- Conclusion and Future Work

FRC CSC RAS & PNRPU

Dessert-2020

## PHYSICAL SOURCES OF SOFT ERRORS

- Nuclear particles and cosmic rays
- An external electromagnetic radiation
- Noise along signal lines (crosstalk)
- Noise on power and ground buses
- Substrate noise



FRC CSC RAS & PNRPU

Dessert-2020

## SOFT ERRORS INDUCED BY NOISES

- They are shorter than soft-errors caused by particle strikes and cosmic rays
- Their appearance frequency correlates with the system clock
- They can cause a potential change in both dual-rail signal parts in different directions

FRC CSC RAS & PNRPU

Dessert-2020

## **QUASI DELAY-INSENSITIVE (QDI) CIRCUITS**

- Features increasing their failure tolerance:
  - Redundant dual-rail and two-phase signal coding
  - \* Two-phase functional discipline
  - Indication of all switch completion
- Penalties:
  - Hardware redundancy, especially in combinational circuits
  - Increased signal amount

FRC CSC RAS & PNRPU

Dessert-2020

## **QDI CIRCUIT INDICATION**

#### **Fail-safe indication**

X	XB	State	Indicator
0	0	null spacer	0
0	1	Bit "O"	1
1	0	Bit "1"	1
1	1	unit spacer	0

## **Opposite spacer as a result of the soft error is considered to be another correct spacer**

FRC CSC RAS & PNRPU

Dessert-2020

## **QDI CIRCUIT INDICATION**

#### **Dual-rail indication circuitry basis**





## XOR on standard cells

XOR on CMOS transistors

FRC CSC RAS & PNRPU

Dessert-2020

## NOISE FAILURE NATURE

#### Crosstalk between "victim" trace (X) and "aggressors" (A1, A2)





**Dual-rail "victim" {X,XB}** 

#### Single "victim", X.

FRC CSC RAS & PNRPU

Dessert-2020

### **POSSIBLE SOFT ERRORS**

##	Dual-ra	Valid spacer	
	Before soft error	After soft error	
1.	00	01	null
2.	00	10	null
3.	00	11	null
4.	01	00	null / unit
5.	01	11	null / unit
6.	10	00	null / unit
7.	10	11	null / unit
8.	11	00	unit
9.	11	10	unit
10.	11	01	unit

FRC CSC RAS & PNRPU

Dessert-2020

## **QDI PIPELINE**

C-elements acknowledge pipeline stage switching completion and make previous register phase control



FRC CSC RAS & PNRPU

Dessert-2020

#### **One bit implementation**



## Traditional solution

Failure-safe solution masking state that is opposite to spacer

Dessert-2020

11 of 20

FRC CSC RAS & PNRPU

It is not enough to indicate "anti-spacer" as spacer, because it dead-locks register bit!



FRC CSC RAS & PNRPU

Dessert-2020

## Pipeline register bit circuit protected from stuck-at "anti-spacer"



FRC CSC RAS & PNRPU

Dessert-2020

#### Modified semi-static C-element circuit with null spacer



FRC CSC RAS & PNRPU

Dessert-2020

#### Modified static C-element circuit with null spacer



## Modified C-elements prevent dead-locking pipeline register bit at "anti-spacer"!



FRC CSC RAS & PNRPU

Dessert-2020

## **QDI-PIPELINE TOLERANCE**

**QDI-pipeline tolerance to the soft errors induced by noise:** 

- Non-protected typical register bit 82.1%,
- Register bit masking "anti-spacer" 86.3%,
- Register bit masking "anti-spacer" and self-repairing stuck-at "anti-spacer" – 97.8%

FRC CSC RAS & PNRPU

Dessert-2020

## CONCLUSIONS

- Strict adjacent placement of the dual-rail wires on the layout makes the most critical soft error type, which is the data token inversed to the current or expected one, not feasible
- Indication of AS state as a spacer and the use of modified C-element protected against stuck-at AS in the QDI pipeline register bit together provide an increase in QDI pipeline natural immunity up to 97.8%
- Our further work will be devoted to studies of QDI pipeline immunity to the soft errors induced by noise for various circuits of the pipeline stage register and handshake control between pipeline stages

FRC CSC RAS & PNRPU

Dessert-2020

# Thanks!

FRC CSC RAS & PNRPU

Dessert-2020

## CONTACTS

- Address: Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of Russian Academy of Sciences (IPI RAS), Russia, 119333, Moscow, Vavilov str., 44, building 2
- Director: academician Sokolov I.A.
  - Tel.: +7 (495) 137 34 94
  - Fax: +7 (495) 930 45 05
  - E-mail: ISokolov@ipiran.ru
- Speaker: Kamenskih A.N., YStepchenkov@ipiran.ru

FRC CSC RAS & PNRPU

Dessert-2020