CELL LIBRARY FOR SPEED-INDEPENDENT VLSI

Stepchenkov Yuri, Zakharov Victor, Rogdestvenski Yuri, Diachenko Yuri, Morozov Nickolai, Stepchenkov Dmitri

Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences, IPI RAS, Moscow, Russian Federation

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Main features of SI-circuits

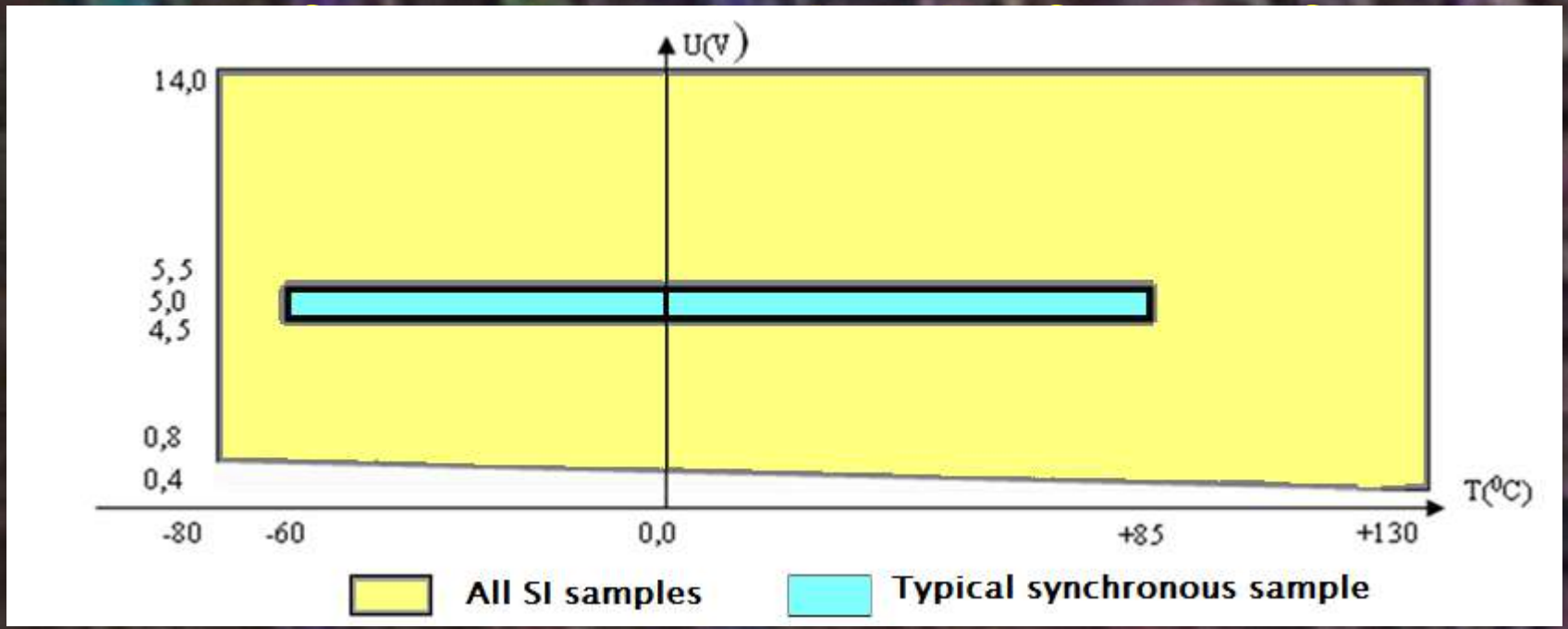
Speed-Independent (SI) circuits excel synchronous ones in:

- Robustness to variation of electrophysical parameters or to their degradation
- Operation safety and validity of the data processing results
- High performance, that is maximum possible at any real environment and data

Experience in SI-circuits

4-Bit Microcontroller core (*analog of PIC18*)

- Complexity is greater by factor of 1.43,
- Workability range (S=ΔU*ΔT) is wider by factor of 16,



Peculiarities of SI-circuits

- Two-phase discipline: work and spacer (pause)
- Indication of each operation phase
- Acknowledge-require technique of interaction between SI-units
- An arbitrary duration of each phase

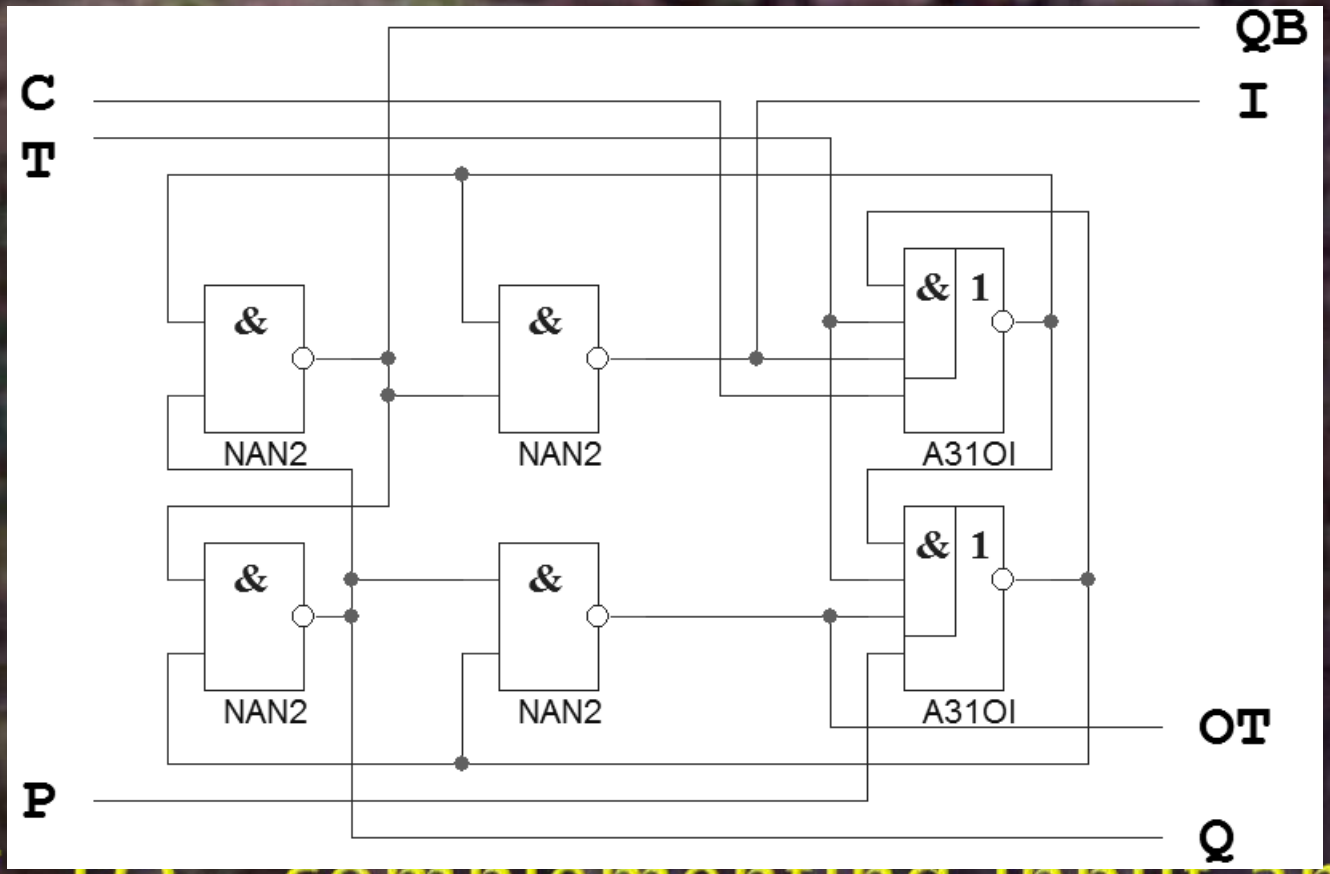
Specific circuit base for SI-units

- All cells for designing SI-circuits must be single-stage one or have an output indicating all interior signals
- Their inputs and outputs take only logical 0 and 1 values

Library's content

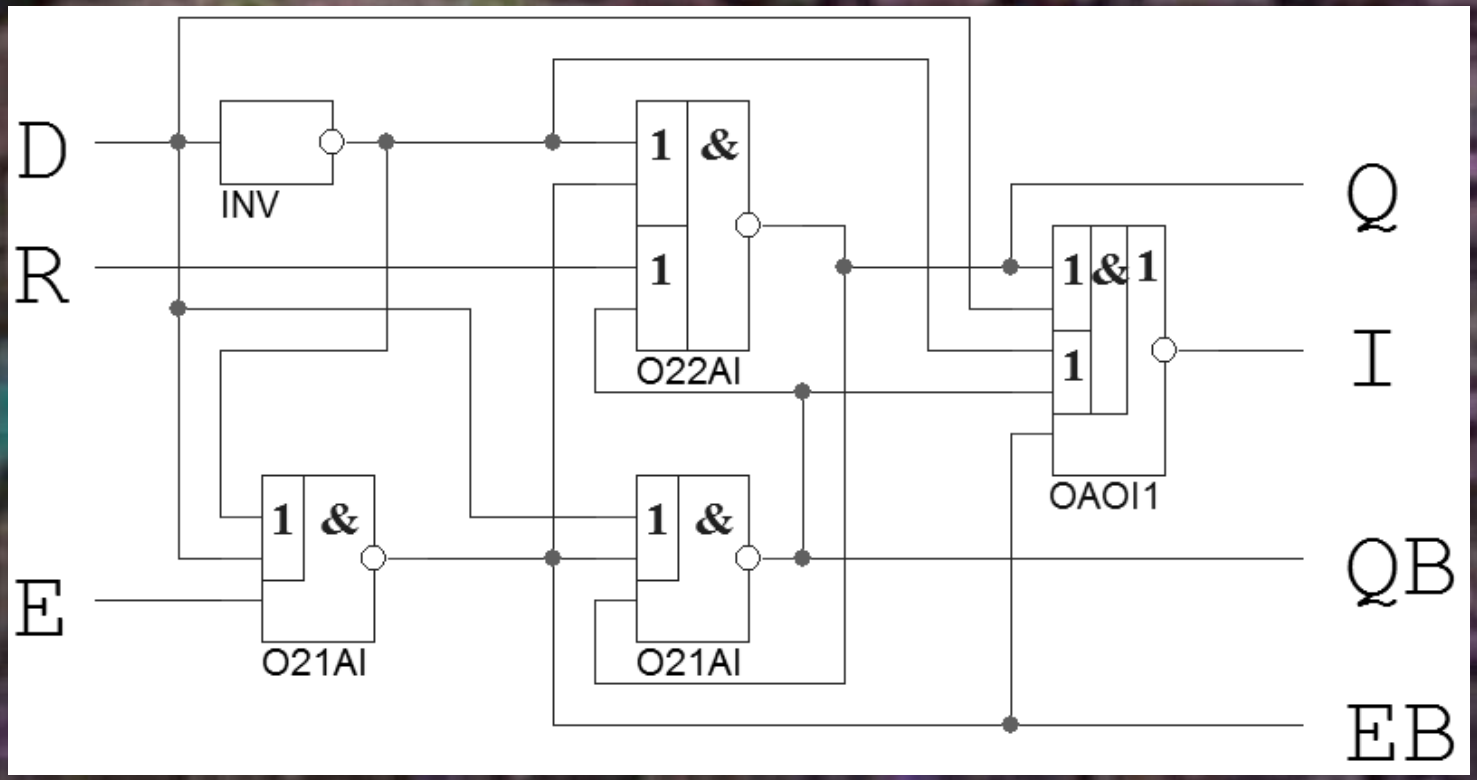
- Combinational logic
- Triggers
- Counters
- Multiplexers
- Adders
- Code converters
- Indicators

Bit of binary counter



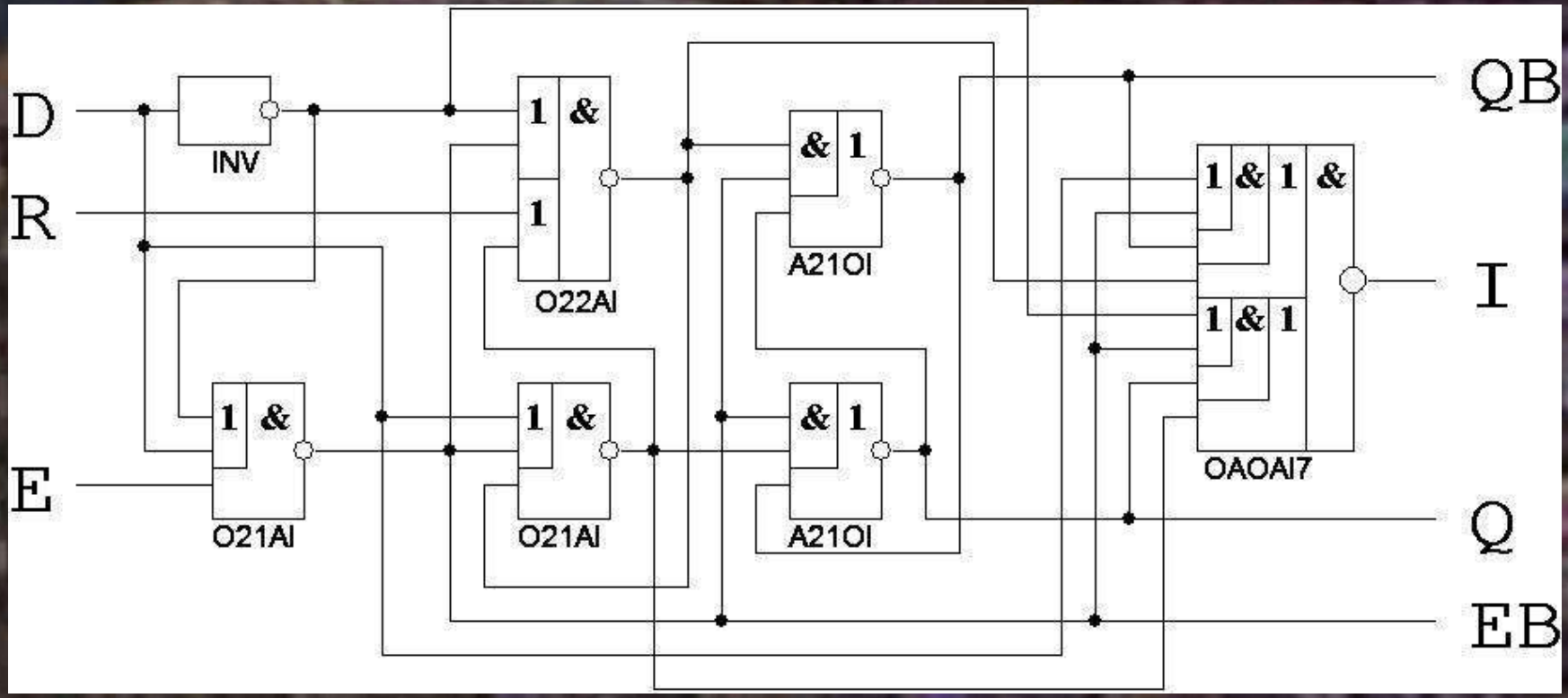
T, TO – complementing input and output; C, P – preset inputs; I – indicator

Interface cells: latch



D – unary data input; E – write enable input with null spacer; R – asynchronous reset

Interface cells: flip-flop



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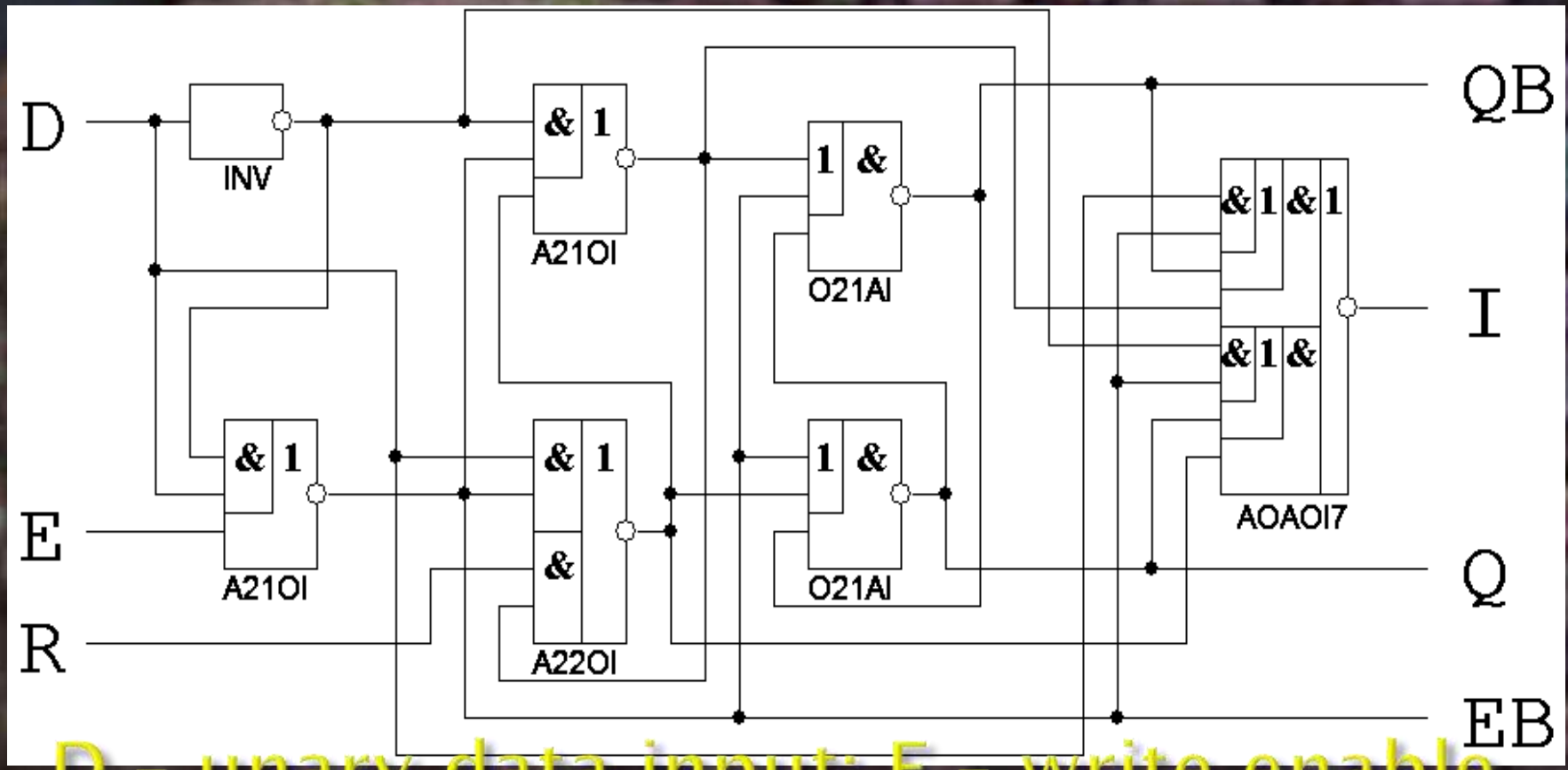
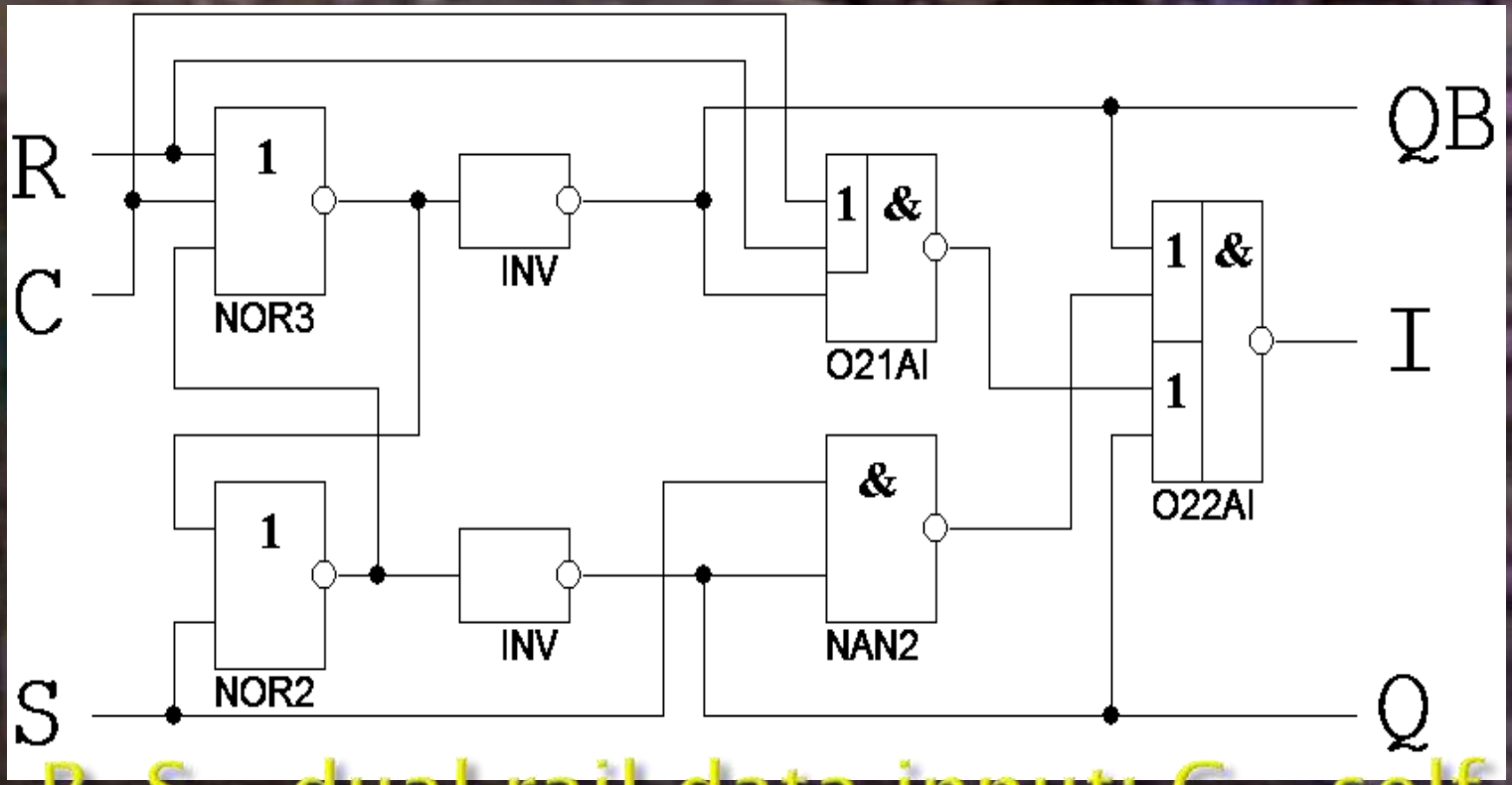


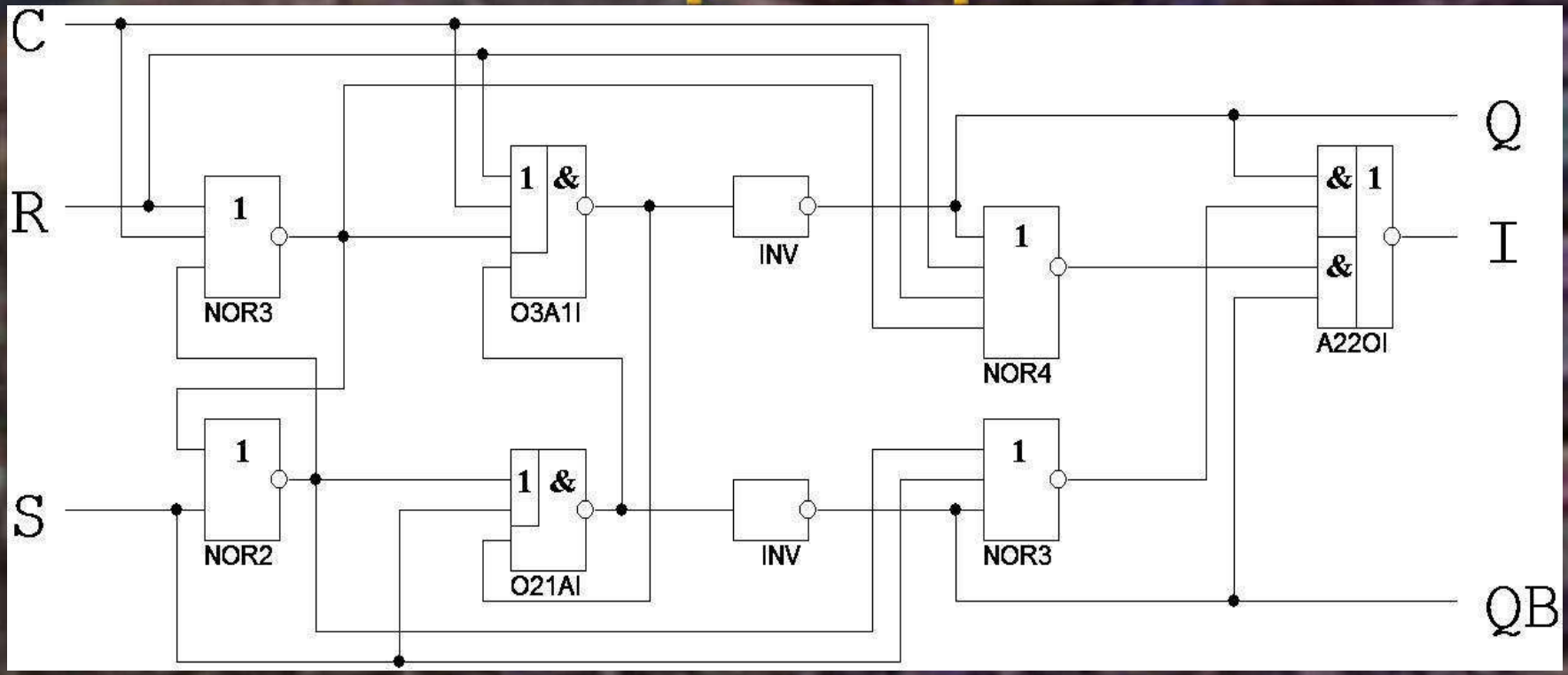
D – unary data input; E – write enable input with unit spacer; R – asynchronous reset

Cells with forced output: latch



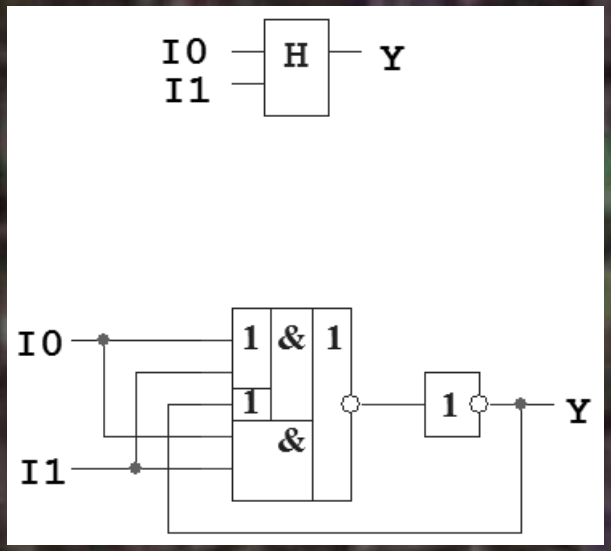
R, S – dual-rail data input; C – self-timed reset; Q, QB – bi-phase forced output

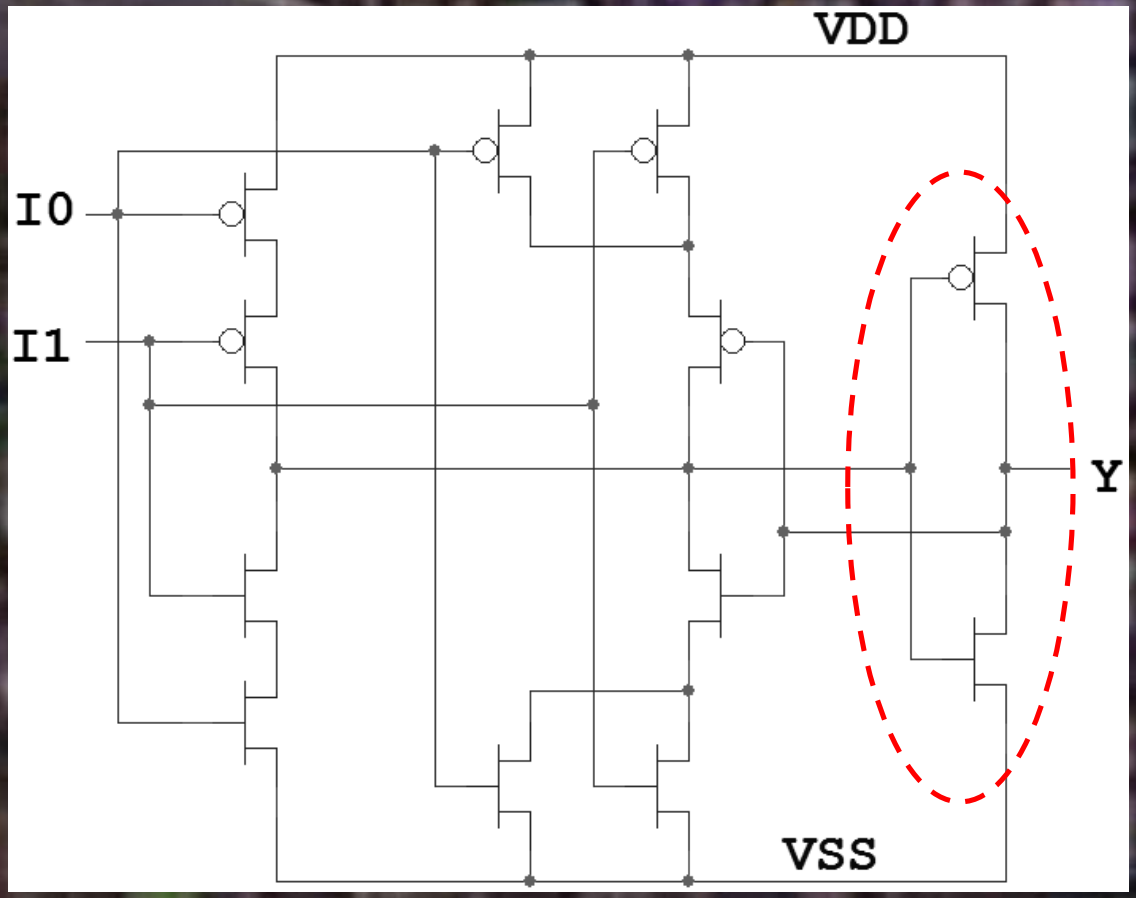
Cells with forced output: flip-flop



R, S – dual-rail data input; C – self-timed reset; Q, QB – forced output

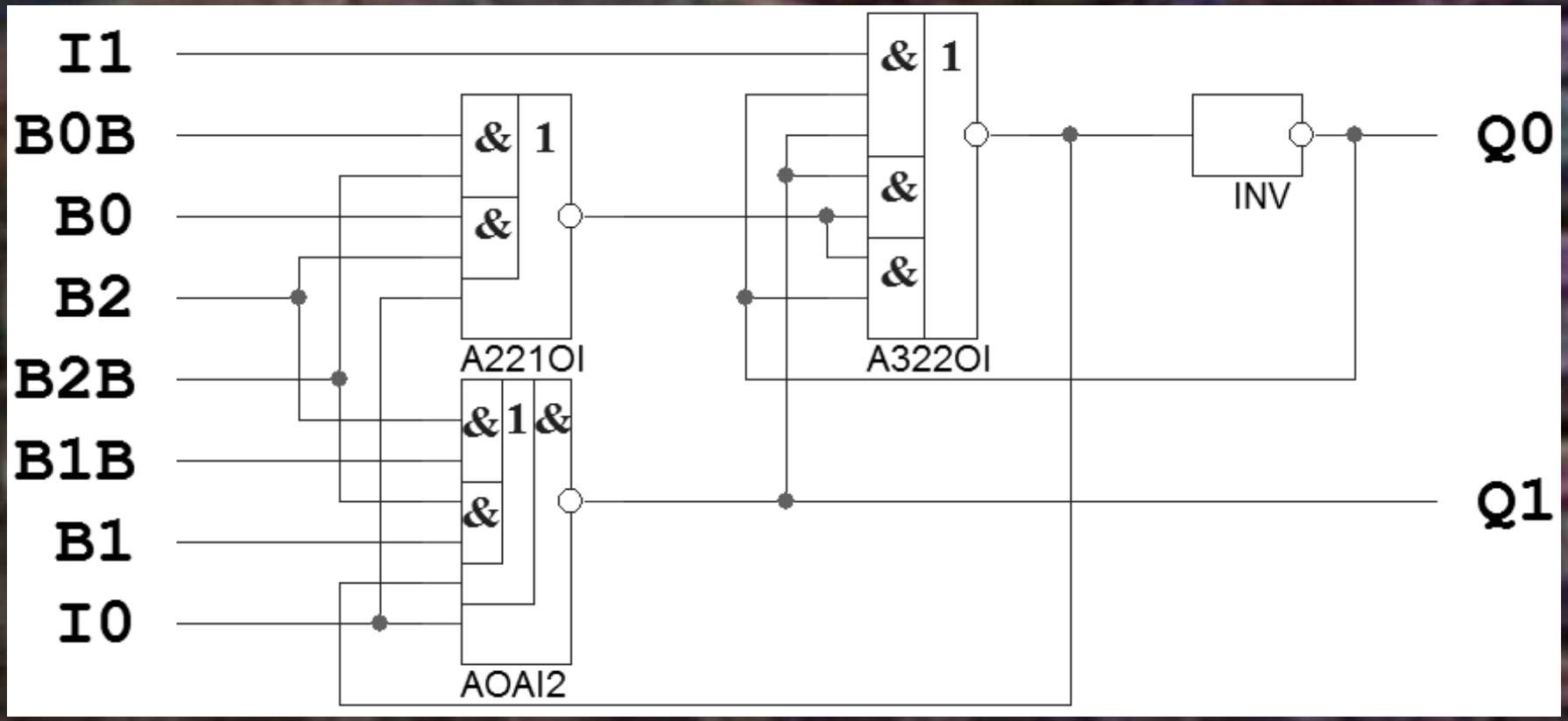
Indication cells: hysteresis triggers





I0, I1 – indication signals

Indication cells: combined logic



I0, I1 – indication signals;
B*,B*B – bi-phase data signals

Library characterization

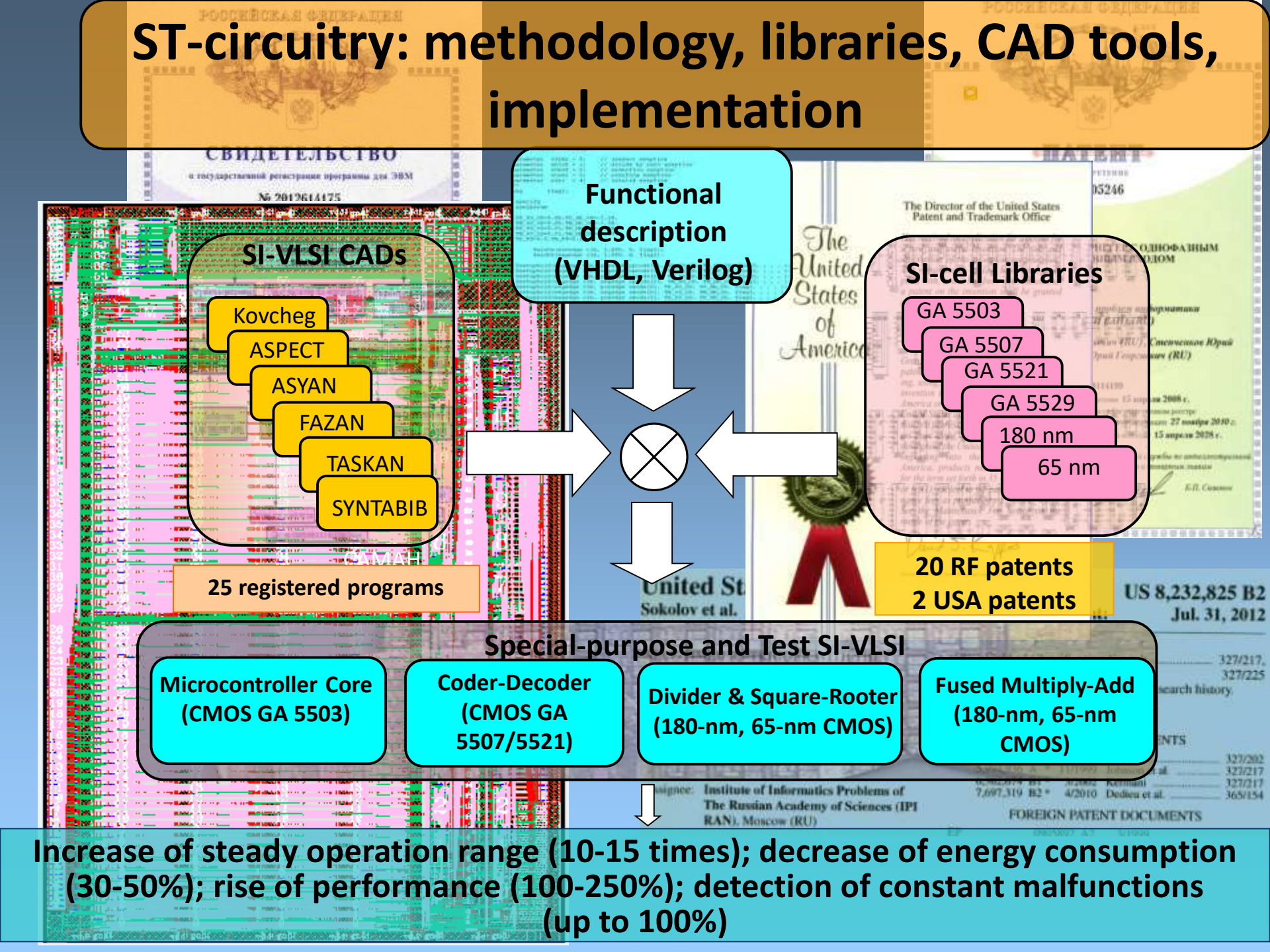
- Self-timed feature analysis (ASPECT)
- Automatic calculation of the electrical and timing parameters (STERH)
- Model files in LIBERTY and Verilog formats (STERH)
- Integration with modern industrial CADs

Cell library approbation

Various CMOS standard processes:

- 1.5 μm for semicustom circuits (Microcore, 14 000 transistors),
- 0.18 μm for semicustom circuits (Microcore, 17 000 transistors),
- 0.18 μm for custom VLSI (Square-Root & Divider, 77 000 transistors),
- 65 nm for custom VLSI (Square-Root & Divider, 77 000 transistors; Fused Multiply-Add Unit, 315 000 transistors)

ST-circuitry: methodology, libraries, CAD tools, implementation



Conclusions

Suggested library:

- **Corresponds to the criteria of building SI-circuits,**
- **Contains more than 200 library cells expanding standard cell libraries,**
- **Provides really SI solutions for interfacing with synchronous environment and for driving large loads**

Thanks!

Contacts

- Director: academician Sokolov I.A.
- Address: Institute of Informatics Problems of the Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences (IPI RAS), Moscow, Russian Federation, 119333, Vavilova str., 44, b.2
- Tel: +7 (495) 137 34 94
- Fax: +7 (495) 930 45 05
- E-mail: ISokolov@ipiran.ru
- Stepchenkov Y.A., tel. +7 (495) 671 15 20, Ystepchenkov@ipiran.ru