Library of functional cells for self-timed GA-VLSI

Stepchenkov Yuri Afanasiaevich, Denisov Andrey Nikolaevich, Diachenko Yuri Georgiyevich, Gavrilov Sergei Vladimirovich, Morozov Nikolai Viktorovich, Stepchenkov Dmitrii Yurievich

> YStepchenkov@ipiran.ru, den@tcen.ru,YDiachenko@ipiran.ru, s.gavrilov@tcen.ru, NMorozov@ipiran.ru, DStepchenkov@ipiran.ru

Abstract

This report is devoted to development of design tools and production of self-timed (ST) VLSI (all possible classes) on the basis of the gate arrays (GA). GA choice, as basis for design of SS-VLSI locates. The structure of library of the elements providing effective design of SS-circuits of various classes on the basis of the GA 5503/5507, 5521/5528 domestic series is described.