ISSN 1063-7397, Russian Microelectronics, 2014, Vol. 43, No. 7, pp. 454–458. © Pleiades Publishing, Ltd., 2014.
Original Russian Text © E.V. Kuznetsov, D.V. Ryazancev, 2013, published in Izvestiya Vysshikh Uchebnykh Zavedenii. Elektronika, 2013, No. 4(102), pp. 18–23.

Modeling of the Secondary Breakdown in a Lateral DMOS Transistor by Irradiation

E. V. Kuznetsov and D. V. Ryazancev

NPK Tekhnologicheskii Tsentr, Moscow, Russia

e-mail: D.Ryazancev@tcen.ru

Received August 28, 2012

Abstract—Using numerical modeling, we have considered the influence of the design-technological parameters of a lateral DMOS-transistor on the resistance to the effect of a secondary breakdown caused by the action of heavy charged particles. Approaches to the optimization of a DMOS-transistor resistant to the action of heavy charged particles are developed. Comparison of the modeling results of the DMOS-transistor's robustness with the experimental data has been carried out.

DOI: 10.1134/S1063739714070117

INTRODUCTION

In recent years, silicon lateral MOS-transistors with double diffusion (DMOS) are widely employed in SHF-equipment in the frequency range of 3–5 GhZ in circuits of power amplification [1] and as power transistors integrated with analog-digital CMOP-technology. For DMOS transistors to be used in the equipment designated for aerospace and the military, they should be radiation-resistant and robust against the action of heavily charged particles (HCPs) of cosmic rays. It is known [2, 3] that HCPs cause two effects in power MOS-transistors: the breakdown of the gate insulator (effect Single Event Gate Rupture) [4, 5] and the secondary breakdown of the transistor (effect Single Event Burnout) [6, 7]. It was shown in [8] that the design of a DMOS-transistor ensures its robustness against the effect of the breakdown of the gate insulator.

In this work we present the results of the investigation into the effect of a secondary breakdown in a DMOS-transistor using the technique of mathematical modeling.

As a result of modeling, a mechanism is revealed which is typical for vertical DMOS-transistors (Fig. 1a) [7]. A heavy particle, when it hits the device structure,

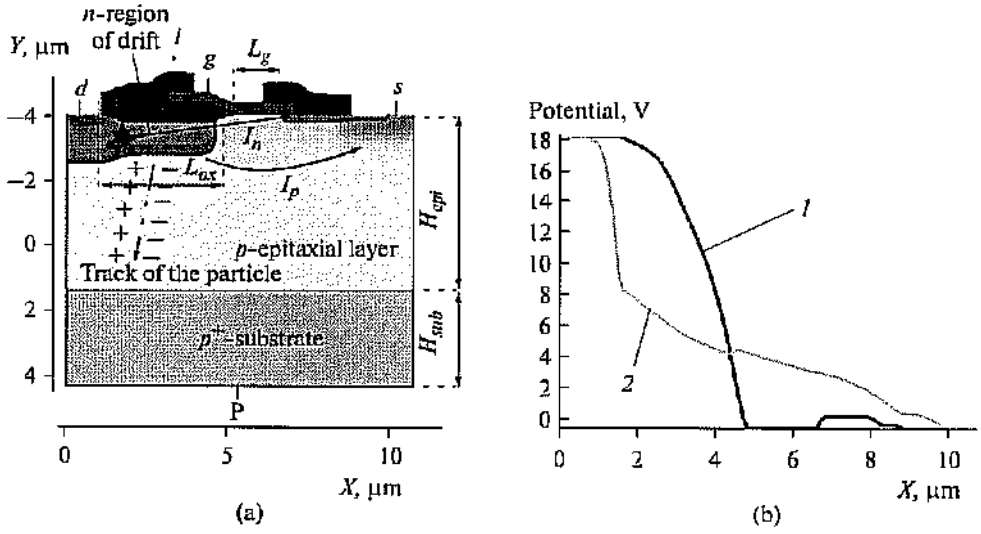

Fig. 1. Parametrized structure of a DMOS-transistor after HCP-hit with combined contacts of source and substrate of (a) and potential distribution in the cross section at point $Y = -3.8$; curve *1* is the potential distribution prior to the HCP-hit, curve *2* is after the HCP-hit (b).

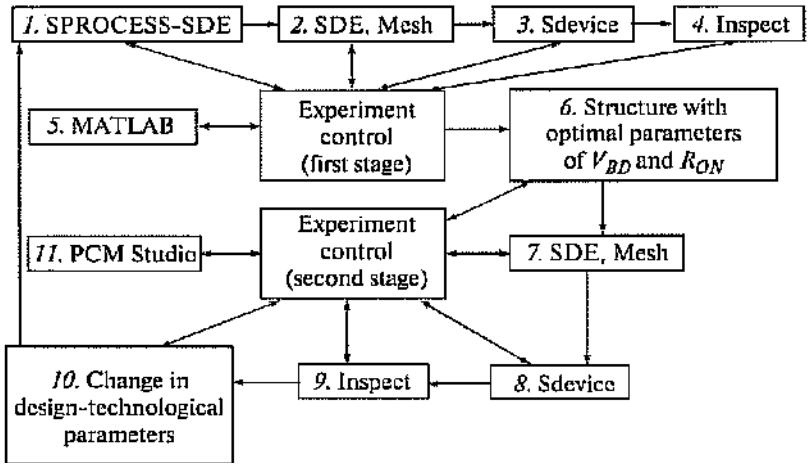

Fig. 2. Structural scheme of studies of the effect of radiation-induced secondary breakdown: (*1*) variation of structure parameters for optimization, in order to obtain optimal pair of breakdown voltage V_{BD} and the resistance in an open state R_{ON}; (*2*) generation of finite-difference net and profiles of impurity distribution; (*3*) calculation of the electrophysical parameters of a physical structure; (*4*) analysis and calculation of V_{BD} and R_{ON}; (*5*) searching for the smallest resistance of R_{ON} at a definite voltage V_{BD}; (*6*) structure with optimal parameters V_{BD} and R_{ON}; (*7*) generation of finite-difference net and profiles of impurity distribution; (*8*) HCP-hit onto the structure of a transistor by varying LEL and drain voltages; (*9*) analysis of the current in the circuit of drain–source and calculation of the presence/absence of HCP-effect; (*10*) change in the design-technological parameters of a DMOS-transistor structure; (*11*) determination of the sensitivity of the parameters to the HCP-effect.

generates electron-hole pairs in it. Due to the presence of a gradient of concentrations of charge carriers and under the action of electric fields, drift and diffusion, respectively, electron I_n and hole I_h currents are formed. The obtained hole current is directed to the contact of the substrate and promotes a forward bias of the p–n-junction of the source–substrate and the injection of electrons (Fig. 1b). The electrons in their movement to the drain enhance the process of impact ionization and promote the formation of avalanche charge multiplication. The hole current I_p formed as a result of the multiplication of the avalanche charge in the drain region results in a further electron injection (I_n) from the source contact. As a result, a positive feedback arises with the participation of a spurious bipolar transistor (n-drain–p-substrate–n-source), which results in the unlimited growth of the current in the circuit source–drain and in the effect of a radiation-induced secondary breakdown. The latter substantially depends on the voltage at the drain, which forms the electric field in the structure directly determining the process of impact ionization and is mostly typical for a transistor in a disabled state. In order to increase the device's robustness to the effect of the secondary breakdown, it is necessary to reduce the transmission gain of a bipolar transistor and the resistance of the substrate body. This is achieved by a decrease in the thickness of the epitaxial layer H_{epi} (as a result, the amount of ionized charge decreases due to its recombination in a strongly doped substrate H_{sub}) and introduction of a highly-doped p-region near the source (p-sinker-region). An increase in the transistor channel length L_g and the length of n-region of drift L_{nx} also results in an increase in the thickness of the base of a bipolar transistor and decrease in the current transmission gains. However, in this case, the operational characteristics of a DMOS transistor substantially deteriorate.

Thus, the problem of transistor optimization is reduced to searching for a design which can provide the maximum possible operating characteristics at a preset level of robustness to the HCP effect.

DESCRIPTION OF TECHNIQUE

In order to study the effect of the secondary breakdown and optimizing the structure of a DMOS-transistor, a technique making it possible to carry out numerical experiments is developed at SAPR TCAD Sentaurus. A structural scheme of the study conditionally composed of two stages is presented in Fig. 2.

At the first stage, a possibility is envisaged to form the structure and its subsequent optimization without accounting for robustness against HCPs. Such an optimization, which is usually applied by developing power MOS-transistors, consists in searching for a structure with the minimal resistance of the transistor in an open state R_{ON} at a preset value of the breakdown voltages' drain–source V_{BD}. An algorithm of searching for optimal values is fulfilled with the use of the modulus implemented in the software package MATLAB. A parametrized structure of a DMOS-transistor is formed with the help of a bundle of utilities of the physical technological modeling Sentaurus Process

and the designer of Sentaurus Device Editor (SDE) structures. This allows us to achieve a more efficient employment of the machine resources.

At the second stage, the optimized structure is studied in terms of its resistance to the effect of the secondary breakdown. In order to simulate the effects of HCPs, a model of a heavy ion [9] is introduced into the Sentaurus Device utility, in which the rate of generation of the secondary charge caused by the HCPs is calculated according to the formula

$$G(l,w,t) = G_{LET}(l)R(w,l)T(t),$$

if $l < l_{max}$ (l_{max} is the length of the track resulting from HCP) otherwise $G(l,w,t) = 0$.

For a spatial charge distribution $R(w,l)$, The Gauss function of distribution is used:

$$R(w,l) = \exp\left(-\left(\frac{w}{w_l(l)}\right)^2\right).$$

The radius w is determined as the distance normal to the HCP track by its hitting the device structure. The characteristic distance w_l is set to be equal to 70 nm. Function G_{LET} generating the density of linear energy losses (LELs) depends only on the LEL of the particle. This allows us to characterize the effects of single faults depending on the LELs of the particle without accounting for its type and energy. The criterion for the determination by modeling whether the effect of a radiation-induced secondary breakdown is present or absent is an unrestorable increase in the drain–source current, higher than 0.1 μA, when a particle with a preset value of LEL bombards a transistor in a disabled state at the preset drain–source voltage.

The design allows us to achieve both two- and three-dimensional modeling. The latter requires greater calculation resources and time and is unreasonable in a number of cases. The two-dimensional modeling allows us to achieve the worst case (a structure with a large channel width) regarding the resistance to the HCP-effect, because the total generated by a particle charge by two-dimensional modeling exceeds that for three-dimensional modeling at the same density of charge distribution in a semiconductor. In the most critical case, the two-dimensional modeling will correspond to the three-dimensional one at a transistor width smaller than that of the generated charge region due to the HCP-hit, when the charge along the Z axis (width) is not practically changed. The worst situation arises also without the use of the model, which takes into account the temperature of the crystalline lattice and heating of charge carriers by an avalanche multiplication, because with an increase in the temperature, the voltage of the avalanche breakdown increases and it causes an increase in the structure's resistance to the HCP-effect.

If the resistance to the HCP-effect does not meet the preset values, it is necessary to do the following:

—to determine a set of design-technological parameters to suppress the spurious bipolar transistor, which promotes an unlimited growth of the current;

—to choose the range of variations of each parameter from the set, taking into account the most critical values;

—to determine the sensitivity of each parameter with the use of the PCMStudio utility;

—to choose the most sensitive parameters;

—to determine the values of the chosen parameters which enable obtaining the needed transistor robustness against the HCP-effect for specific drain voltages by varying the LEL or for a specific LEL by varying the drain voltages;

—to transfer to the first stage of studies and repeat the structure optimization with a fixed set and values of parameters, in order to find an optimal pair of breakdown voltages and resistance in an open state.

The changed structure of a DMOS-transistor is repeatedly studied for its resistance to the radiation-induced secondary breakdown effect. The process can be repeated many times to obtain the needed transistor resistance. This algorithm makes it possible to obtain the necessary resistance of a DMOS-transistor to the HCP-effect with the maximum possible operating characteristics.

IMPLEMENTATION OF THE TECHNIQUE

The dependence of the drain voltage of a DMOS-transistor on LEL of the particle was studied by designing the 1469KT1T microcircuit, which includes a DMOS-transistor. The described above technique was employed by designing this DMOS-transistor. A minimal resistance in an open state at a breakdown voltage of about 80 V was found at a specific peak concentration and a length of 2.4 μm of the n-region of drift. In accordance with the numerical optimization, test samples of a DMOS-transistor were fabricated. Calibration of physical models employed in calculations was carried out according to the experimental I-V-characteristics and measured electrophysical values for the test samples. Agreement between the experimental and calculated I-V-curves and transistor parameters is achieved.

After optimization, the resistance of a transistor to the secondary breakdown effect was studied at $V_g = 0$ V, $V_s = 0$ V, and $V_d = (14–24)$ V and the voltage at the substrate contact $V_s = 0$ V. By experimental tests of the DMOS-transistor's resistance to the HCP-effect, the width of the transistor was smaller or about the size of the region of the induced charge distribution after bombardment by a HCP; therefore, two-dimensional modeling was chosen.

Figure 3 shows the calculated and experimental dependences of the drain voltage on the LELs of the particle at which the effect of a radiation-induced secondary breakdown does not occur. We will call this

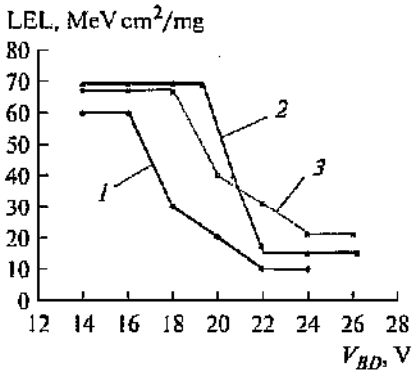

Fig. 3. Calculation and experimental dependences of the boundary drain voltage V_{DB} on LEL of the particle; *1* modeling in SAPR TCAD; *2* experiment (ENPO SPELS); *3* experiment (Universite Catholique de Louvain, Louvain-la-Neuve, Belgium).

voltage as the boundary drain voltage V_{DB} at a given LEL of the particle. A minor difference between the experimental data and modeling results can be associated with the variation of the parameters of the technological operations by the production of devices and with the fact that two-dimensional modeling was used without accounting for the temperature dependences of the breakdown voltage by avalanche multiplication of charge carriers.

The obtained parameters of the transistor's resistance to the effect of radiation-induced secondary breakdown on the results of modeling correspond to LELs equal to 10 MeV cm²/mg at a voltage of 24 V. Using the considered algorithm, a problem is formulated for achieving a transistor's radiation robustness for a drain voltage of 25 V at an LEL of the particle of 60 MeV cm²/mg. These values are necessary for the device's operation in the equipment designed for space.

In order to increase the boundary drain voltage at a given LEL equal to 60 MeV cm²/mg, a list of the parameters which primarily influence this voltage and their sensitivity to this voltage were determined.

Figure 4a shows a graph of V_{DB} for a DMOS-transistor by varying the LEL of the particle at a decline in the thickness of the epitaxial layer H_{epi}, while Fig. 4b shows a similar graph by an increase in the channel length L_g. By a decrease in the thickness of the epitaxial layer, the boundary drain voltage increases at a fixed LEL of the particle compared to the base structure, but the breakdown voltage V_{BD} decreases. An increase in the transistor channel length L_g also makes it possible to increase V_{DB}; however, in this case, the input load capacitance substantially increases.

The presence of a bottom contact to the substrate does not substantially affect the dependence of V_{BD} of a transistor on the LEL of the particle, just as a change in the concentration in the region of the upper contact to the substrate does not substantially affect it.

As a result of the studies carried out, it is revealed that an increase in the drain boundary voltage at LEL of 60 MeV cm²/mg to 25 V is possible by increasing the length of the separating layer of SiO_2 L_{ox} between the drain and channel of a transistor to 6.4 μm and increasing the depth of location of the n-region of the drift to the contact with a strongly doped substrate. In this case, the resistance in an open state increases by up to a factor of 2 at an equivalent breakdown voltage with respect to the base structure with a length n-region of a drift of 2.4 μm.

Thus, the developed in the medium of the device-technological modeling Synopsys Sentaurus TCAD technique of studies and optimization of the design-technological parameters of a lateral DMOS-transistor, taking into account the resistance to the effect of radiation-induced secondary breakdown allows us to obtain at a preset level of resistance the maximum pos-

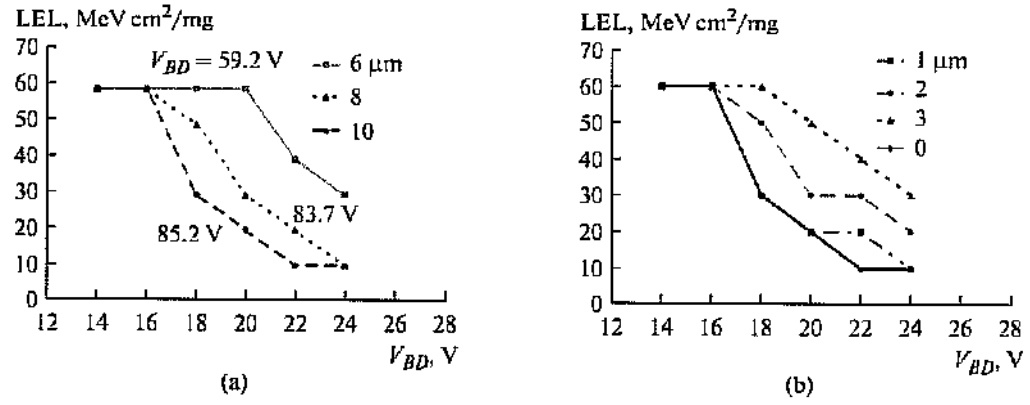

Fig. 4. Dependence of the drain boundary voltage V_{DB} on LEL of the particle by a decline in the thickness of the epitaxial layer H_{epi} (a) and increase in the transistor channel length L_g (b).

sible operating characteristics of the device. The design is verified according to the experimental data.

ACKNOWLEDGMENTS

The work is carried out with the financial support by the Ministry of Education and Science of the Russian Federation using the equipment of the Center of Collective Use "Functional Control and Diagnostics of Micro- and Nanosystem Engineering based on R&D Technological Center" (GK 07.514.12.4025).

REFERENCES

1. Kuznetsov, E.V. and Shemyakin, A.V., Power SHF DMOS-transistors for wireless technologies for data transmission (Review), *Izv. Vyssh. Uchebn. Zaved., Elektron.*, 2009, no. 6 (80), pp. 8–15.
2. Busatto, G., Porzio, A., and Velardi, F., et al., Experimental and numerical investigation about SEB/SEGR of power MOSFET, *Microelectron. Reliab.*, 2005, vol. 45, nos. 10–14, pp. 1711–1716.
3. Chumakov, A.I., *Action of Cosmic Radiation on Integrated Circuits*, Moscow: Radio i svyaz', 2004, 319 p.
4. May, T.C. and Woods, M.H., Alpha-particle-induced soft errors in dynamic memories, *IEEE Trans. Electron Devices*, 1979, vol. ED-26, no. 1, pp. 2–9.
5. Fischer, T.A., Heavy-ion-induced, gate-rupture in power MOSFETs, *IEEE Trans. Nucl. Sci.*, 1987, vol. 34, no. 6, pp. 1786–1791.
6. Waskiewicz, A.W., Groninger, J.W., Strahan, V.H., and Long, D.M., Burnout of power MOS transistors with heavy ions of Californium-252, *IEEE Trans. Nucl. Sci.*, 1986, vol. 33, no. 6, pp. 1710–1713.
7. Johnson, G.H., Hohl, J.H., Schrimpf, R.D., and Galloway, K.F., Simulating single event burnout of N-channel power MOSFET's, *IEEE Trans. Electron Devices*, 1993, vol. 40, no. 5, pp. 1001–1008.
8. Krasyukov, A.U. and Kuznetsov, E.V., Investigation into the effect of breakdown of gate insulator caused by hit of single heavy charged particle in planar power MOS-transistor, *Def. Complex Sci. Tech. Prog.*, 2007, no. 4, pp. 41–46.
9. Sentaurus Device User Guide Version E-2010.12, December 2010.

Translated by Renald Litvinov